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ELECTRONIC DESIGN

30 AUG 1994

MAY 30, 1994

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

EXORCISING DEMONS FROM FAST BOARD DESIGNS

- DAC TACKLES HIGH-LEVEL DESIGN
- MULTIMEDIA INTEGRATION: SPEAKERS AREN'T EASY
- SPOTLIGHT ON 'PLUG-AND-PLAY'
- PEASE PORRIDGE

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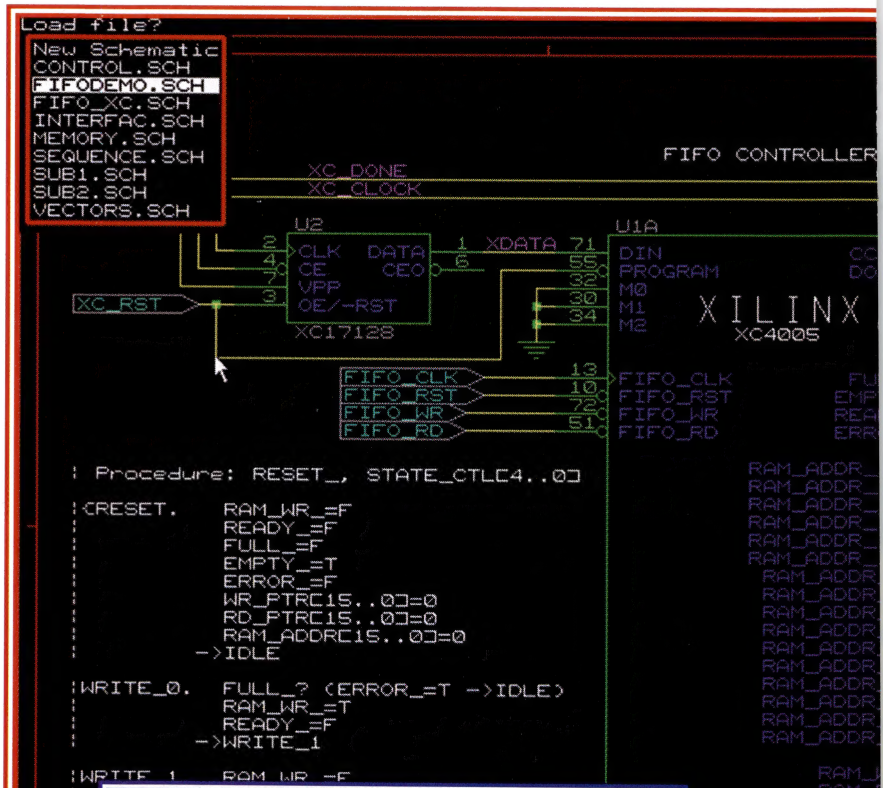
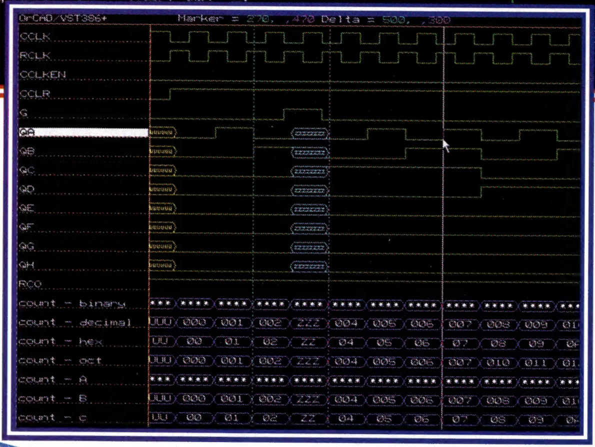
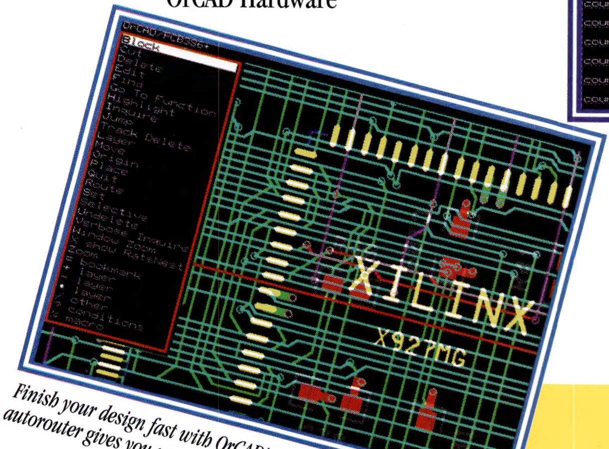


```
Load file?
New Schematic
CONTROL.SCH
FIFODEMO.SCH
FIFO_XC.SCH
INTERFAC.SCH
MEMORY.SCH
SEQUENCE.SCH
SUB1.SCH
SUB2.SCH
VECTORS.SCH
```

```
: Procedure:  RESET_, STATE_CTL[4..0]

:<RESET.      RAM_WR_=F
:             READY_=F
:             FULL_=F
:             EMPTY_=T
:             ERROR_=F
:             WR_PTR[15..0]=0
:             RD_PTR[15..0]=0
:             RAM_ADDR[15..0]=0
:          ->IDLE

:WRITE_0.     FULL_? (ERROR_=T ->IDLE)
:             RAM_WR_=T
:             READY_=F
:          ->WRITE_1

:WRITE_1      RAM_WR_=F
```



(Top) Combine SDT 386+ and PLD 386+ design your boards and the programmal logic devices that populate them. (Left) Design verification is fast ar easy with VST 386+. And, it's supported b Xilinx, Actel, and oth major FPGA vendors.



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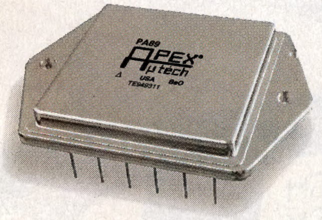
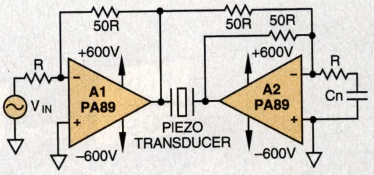


Highest Voltage Supply

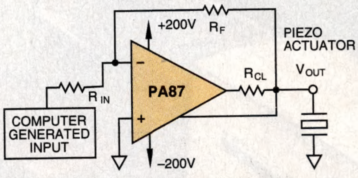
If you're working with supplies of ±75V to ±600V, take a look at the industry's highest voltage power amp—the **PA89**. Output voltages can swing up to 1140V peak to peak with output current up to 75mA.



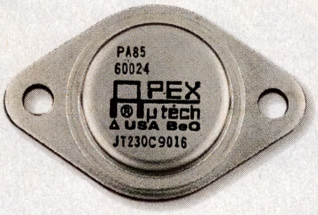
±1100V Single Axis Micro-Positioning

High Output Current

The **PA87** combines a wide supply range of 100V to 450V with its high output capabilities. You'll also be impressed by its low 3mA of quiescent current. Housed in a 10-pin SIP, it's also a low cost solution priced **$52.00** in 10K.

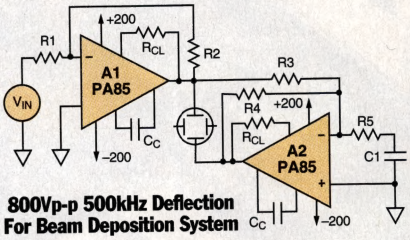


Deformable/Segmented Mirror Actuator

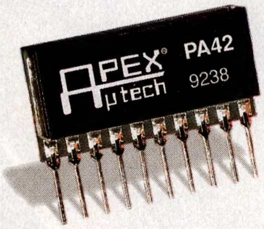


High Speed

If it's speed you need, the **PA85** offers a wide supply range of ±15V to ±225V with a typical slew rate of 1000V/μs. The **PA85** achieves this exceptional speed at a power bandwidth of 500kHz and ±200mA of output current. It's also available in a hi-rel military grade.

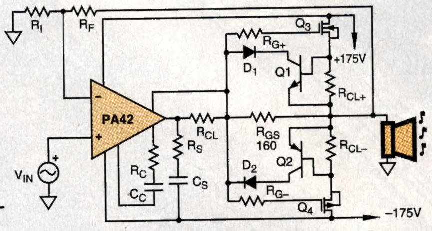


800Vp-p 500kHz Deflection For Beam Deposition System

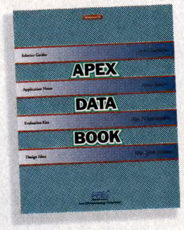


Low Cost Monolithic

The **PA42** is the industry's only monolithic power amp capable of operating on a supply range of 100V to 350V. At **$13.60** in 10K pieces, it's also the industry's lowest cost high voltage power amp. The **PA42** is rated at 120mA of output current and a mere 2mA of quiescent current. Also available in die form.



PA42 With External MOSFETS Creates A Super Power Audio Amp Subwoofer Driver



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KEY PRODUCT SPECIFICATIONS

Part #	V_{SS}	$I_{O\ Peak}$	$I_{Q\ MAX}$	P_D	$/10K
PA89	150V-1200V	75mA	6mA	40W	$269.50
PA87	100V-450V	300mA	3mA	7.5W	$52.00
PA85	30V-450V	350mA	25mA	40W	$82.05
PA42	100V-350V	120mA	2mA	9W	$13.60
PA41	100V-350V	120mA	2mA	12W	$13.60

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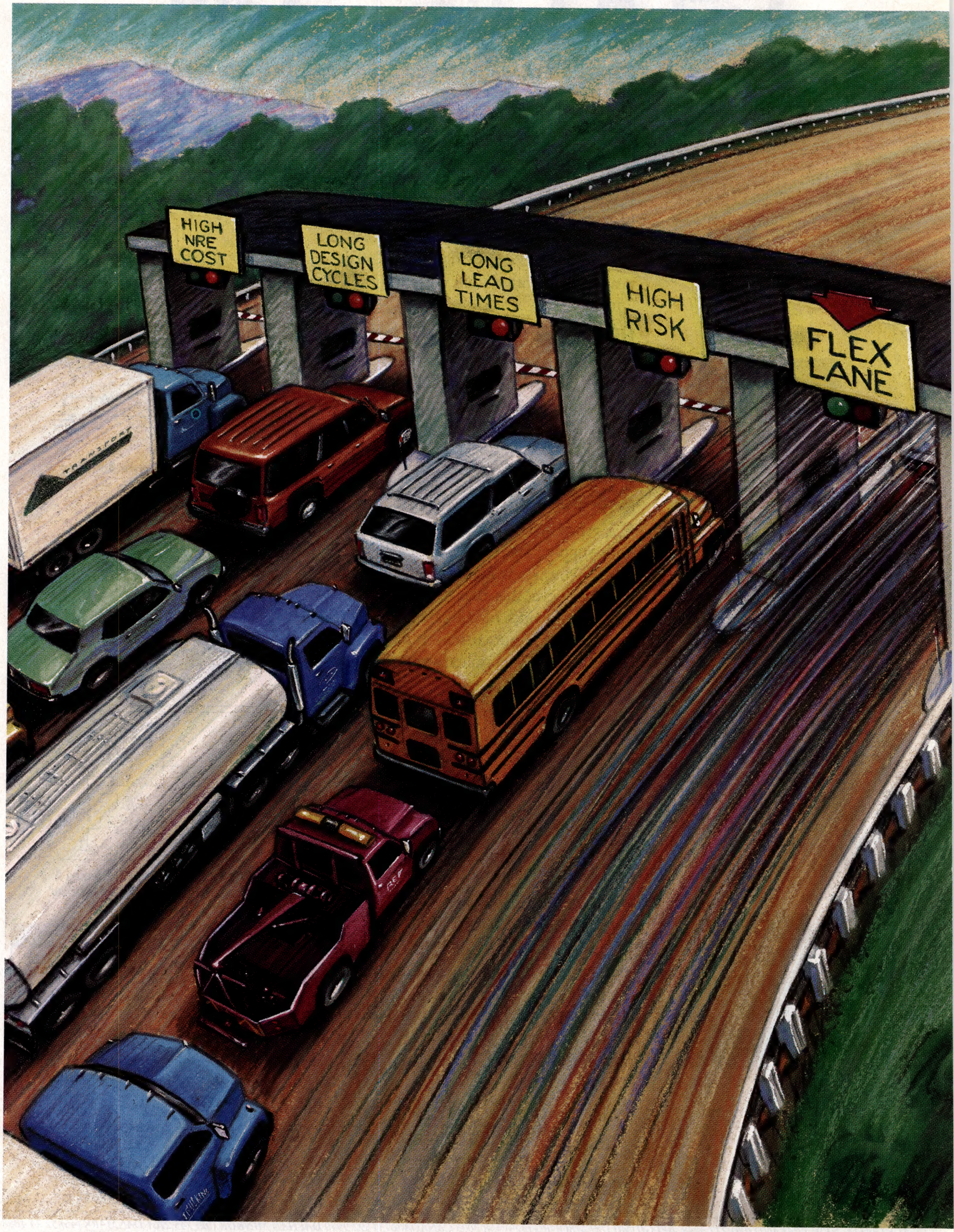

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Production Lead Time	**Off the Shelf**	**8 – 12 Weeks**
Reprogrammability	**Yes**	**No**
In-Circuit Reconfigurability	**Yes**	**No**
Flexibility for Design Changes	**High**	**Low**
Industry Standard CAE Support (VHDL, Verilog)	**Yes**	**Yes**

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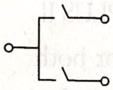
All Units: SOIC 8pin Package

Actual Size



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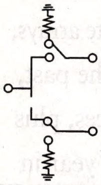
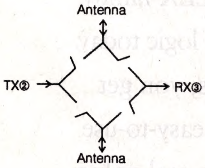


SPDT ABSORPTIVE



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MAY 30, 1994 VOL. 42, NO. 11

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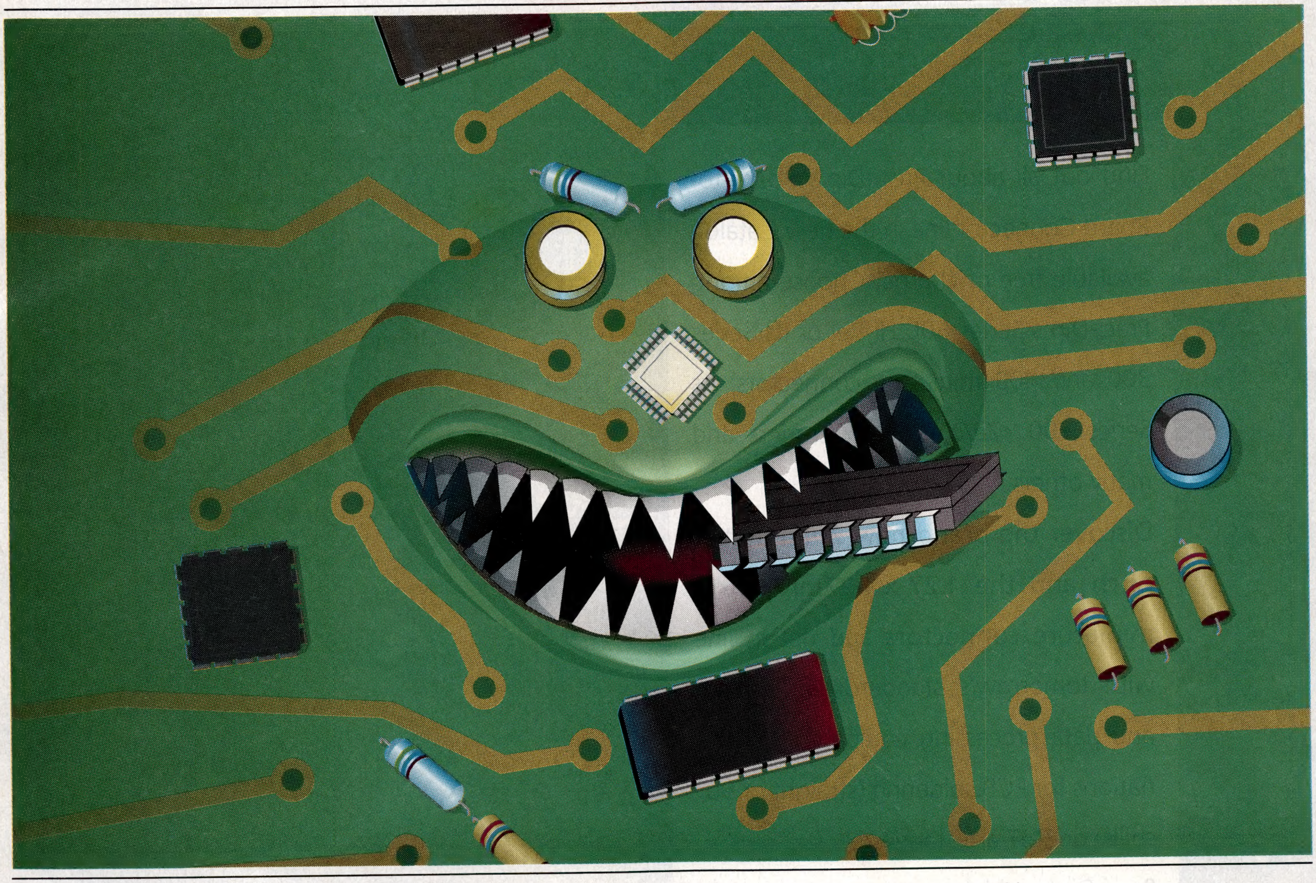

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1980 Certificate of Merit
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- Single-chip PCI interface solutions
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  Ideas for Design
  QuickLook

Correction:
On p. 162 of the April 18 issue, we inadvertently used a photograph of the Maxwell SI Eminence RCS plot from Ansoft Corp. in the New Product story on the ContecPlane from Contec Microelectronics USA.

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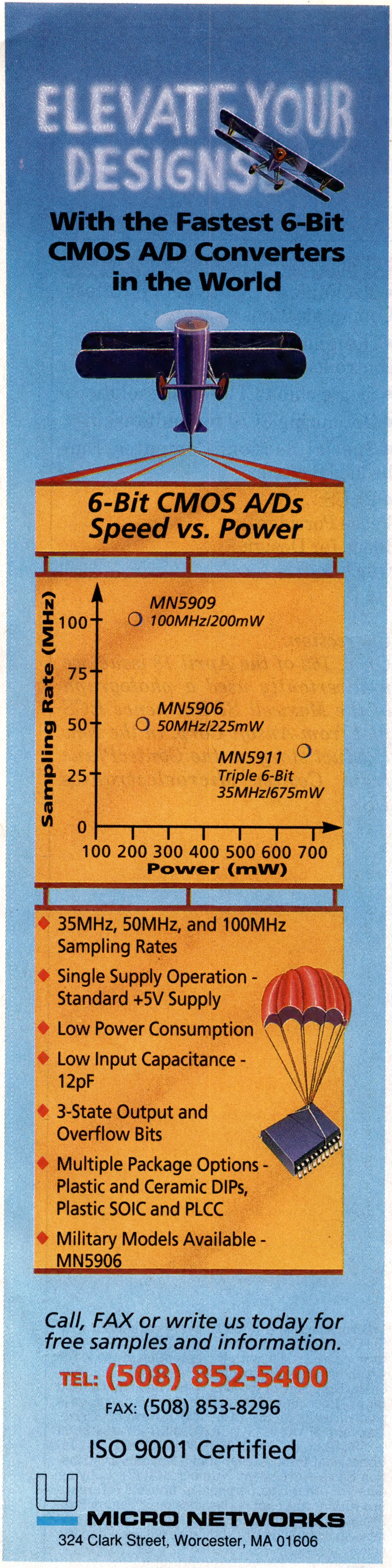

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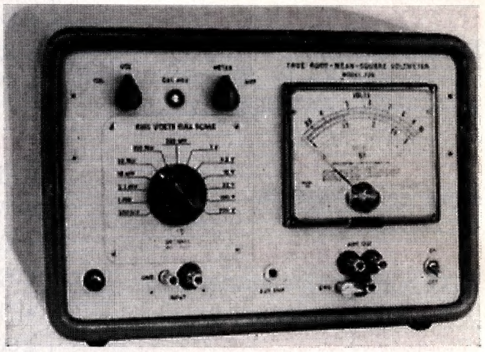
ELECTRONIC DESIGN 40 YEARS AGO

RMS voltmeter measures complex waves

The Model 320 True RMS Voltmeter is an instrument of the ultra-sensitive type to measure true root-mean-square values of highly complex wave forms in addition to sinusoidal waves. It operates over a range of 100µv to 320v and a band of 5cy to 500kc. Accuracy is better than 3% between 15cy and 150kc for any reading regardless of scale position. Other features include a 10 megohm input impedance, a provision for simultaneously observing the voltage reading and monitoring the amplified signal with phones or a CRO, and a built-in calibrator unit for correcting the effects of advanced aging of tubes. Accessories are available for extending voltage range to 20µv and 10kv, and for measuring rms currents from 0.1µamp to 10amp. Ballantine Laboratories, Inc., Dept. ED, Boonton, N.J. *(Electronic Design, May 1954, p. 49.)*



Ballantine Labs excelled in designing true-rms meters, and the company, now based in Cedar Knolls, N.J., still makes them. A question in definitions trivia: Note the use of the term "CRO." At that time, did it stand for "cathode-ray oscilloscope," as one might initially suppose, or did it stand for "cathode-ray oscillograph?" My guess is the latter.—SS

New Books: Magnetic Amplifier Circuits, By William A. Geyger, 277 pages, McGraw-Hill Book Co., Inc., $6.00.

Written for the circuit designer, this book presents the fundamental principles, characteristics, and applications of the magnetic amplifier type of circuit. It covers the basic as well as more complex circuits and emphasizes experimentally observed phenomena without going into extended mathematical considerations and proofs. Descriptive and graphical methods are widely employed for qualitative and quantitative interpretation.

The first chapter presents a classification of saturable-core devices and reviews the history of magnetic amplifiers. Chapter 2 describes magnetic core materials, various types of core construction, winding arrangements, and various types of rectifiers employed in magnetic amplifier circuits. There follows in Chapters 3 to 16 a discussion of the numerous kinds of magnetic amplifier circuits including nonfeedback circuits, single-stage and multi-stage circuits with internal or external feedback, and special circuits that make use of critical regeneration or derivative feedback. The last two chapters cover the technical properties, transient response, and typical applications of magnetic amplifiers, particularly those in instrumentation, servo-mechanisms, regulators, and automatic control devices.

The numerous references at the end of each chapter include many important European patents which have not been discussed in previous presentations of the magnetic amplifier art, according to the author. Engineers working in this field will find the detailed information presented useful in solving special problems. *(Electronic Design, May 1954, p. 76.)*

Magnetic amplifiers were interesting animals, a hot topic back in the 1950s. With their saturable-reactance cores, these solid-state devices could control lots of power, work in extreme environments, and also sum signals that had to remain electrically isolated. For a while, they were a main-line technology—according to the 1975 edition of the ITT "Reference Data for Radio Engineers," mag amps enjoyed their maximum prominence in power-control systems from about 1947 to 1957. But then semiconductors began to take over, and although new transistor-magnetic core circuits were developed, interest waned in magnetic amplifiers.—SS

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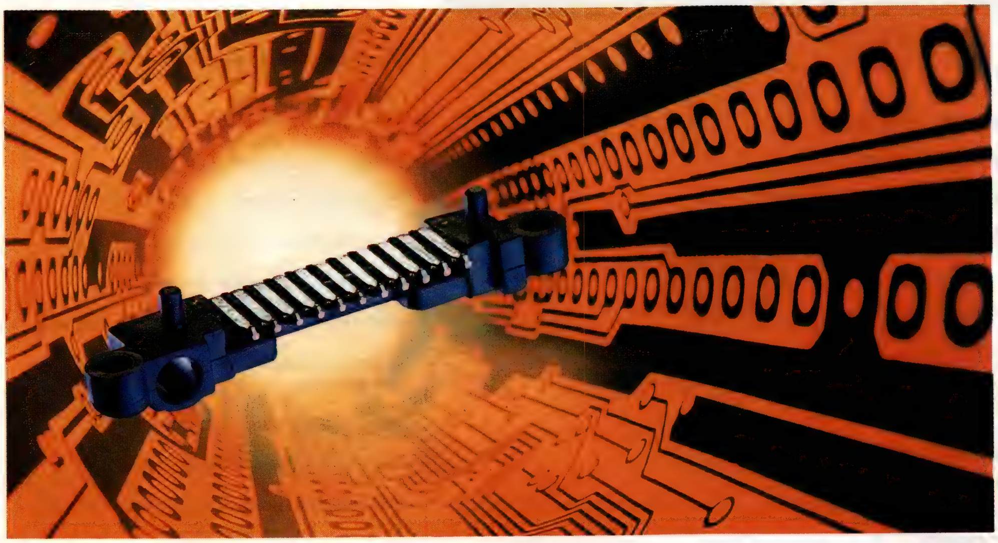

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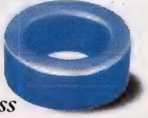

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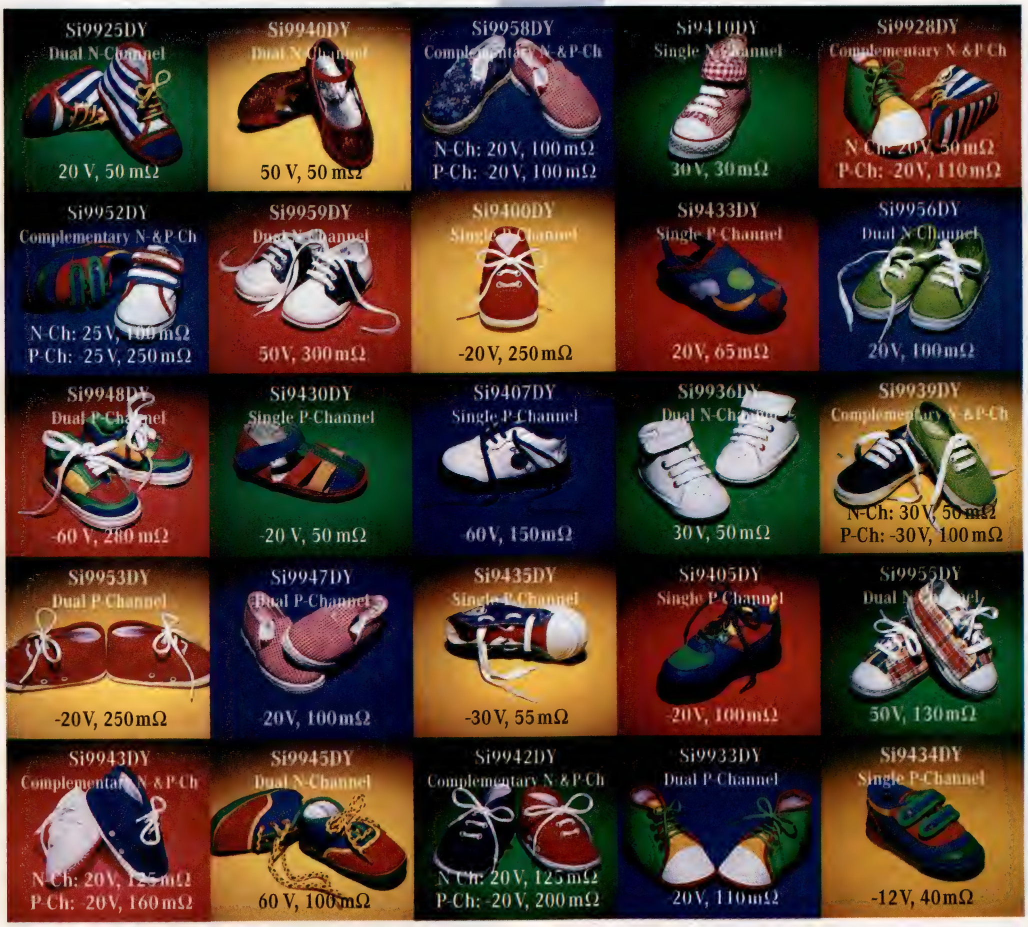

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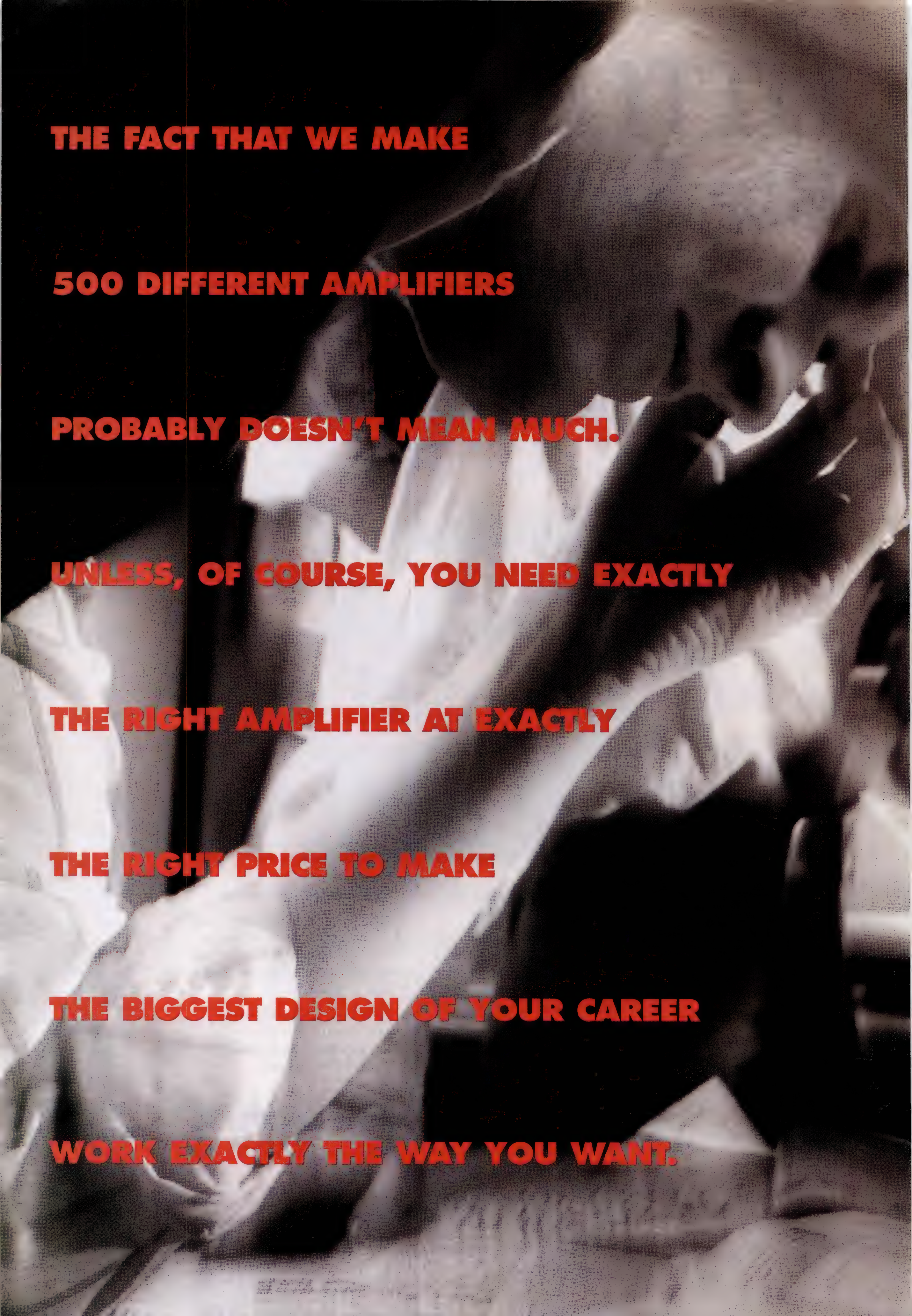
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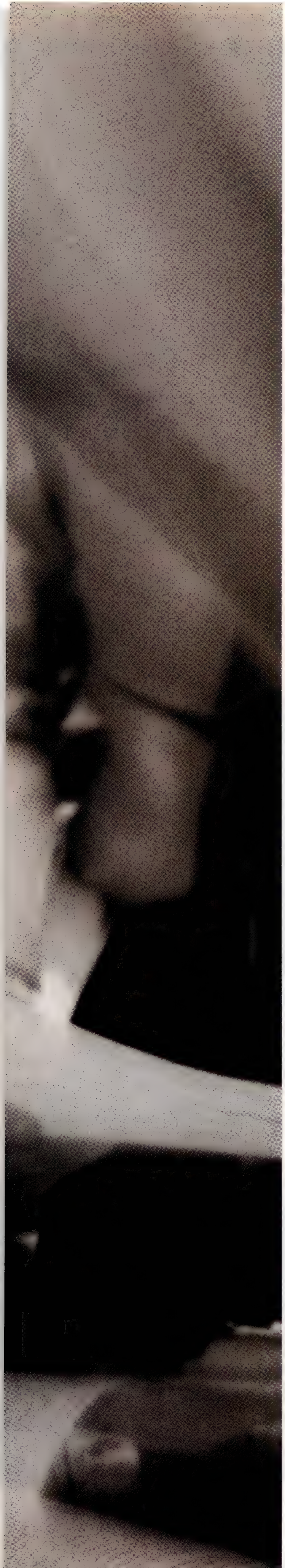

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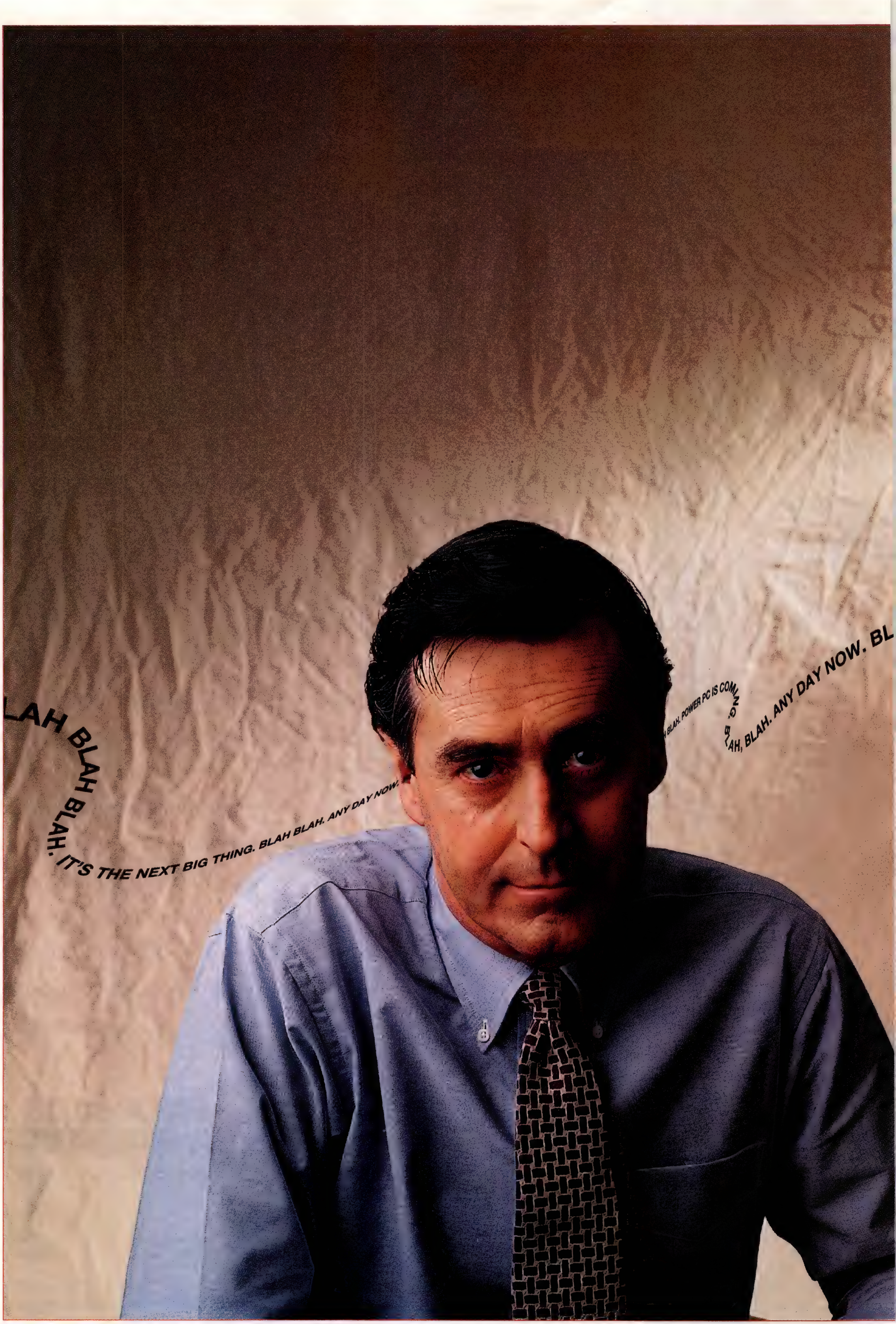
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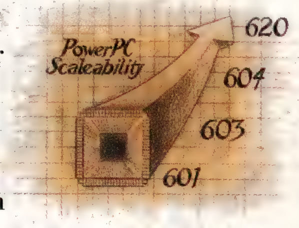

Of course, our momentum isn't confined to products. Today, PowerPC processors are poised to run such popular operating systems as AIX,® OS/2,® Solaris,® System 7, Windows* and Windows NT,™ plus Taligent. In the not-so-distant future, PowerPC adopters can also look forward to the PowerOpen™ Environment (POE), a next-generation, standards-based platform.

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DEFENSE CONVERSION

It's not very often that I look to Washington D.C. for a mental boost, but occasionally I'm pleasantly surprised. A bill recently emanating from the U.S. House of Representatives Committee on Science, Space and Technology, for example, more or less made my day.

One of the United States' greatest resources is its national laboratories system. Long an almost exclusive client of the national defense industry, the work at the labs is slowly being refocused. We often hear about the mission changing from defense to commercial applications. I think it's more accurate to say that the shift is from military-defense to economic-defense R&D.

The bill, which is known officially as the Department of Energy Laboratory Technology Act, addresses some basic issues. These include mandating the Department of Energy to work up a mission statement, a technology road map, and a plan to coordinate the work in the various labs.

Although essential, I think of these goals as being an expression of good intentions. The more practical paragraphs dealing with technology transfer caught my attention. Section 7, for example, requires that the energy department and the labs seek advice from industry on planning for its projects. This becomes a means, therefore, to integrate the technology road map of industry with the work the labs undertake down the line.

One of the great pitfalls in moving from a military defense structure to a economic defense structure is destroying the lines of communication between laboratory and client. When the Department of Defense was the client, it was quite clear that the DOD and the labs could communicate. It's not quite as clear how that will work when commercial enterprise is the client. Establishing lines of communication will take some thought and effort.

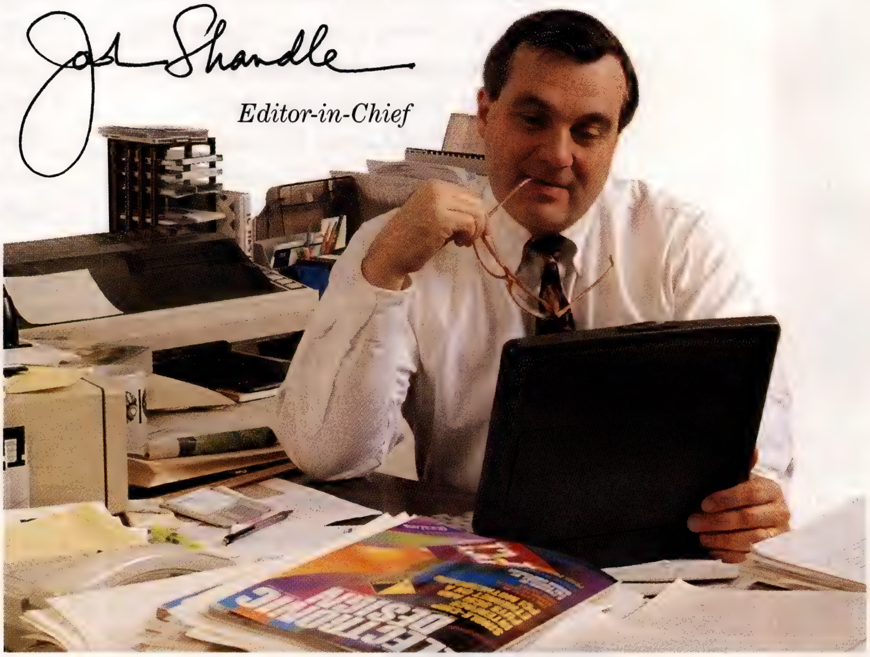
But all in all, it's encouraging to see Congress recognize that industries have technology road maps and that the labs must be in step with them.

I'm also pleased that the most vexing problems of the Cooperative Research and Development Agreements (CRADAs) are being addressed in HR 1432. CRADAs are basically a good idea: companies and national labs working together on a precompetitive technology. There was just too much bureaucracy.

The act would require the Department of Energy to process proposals within 30 days. It would also let the labs enter agreements of less than $500,000 without permission from Washington.

Jack Shandle

Editor-in-Chief



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	HY5116400A	5V	50/60/70	L, 2K/4K, WPB, SR	Q3, 94
	HY51V16400A	3.3V	60/70/80	L, 2K/4K, WPB, SR	Q3, 94
×8	HY5116800	5V	70/80/100	L, 2K/4K, WPB	Q3, 94
	HY5116800A	5V	60/70/80	L, 2K/4K, WPB, SR, EDO	Q4, 94
	HY51V16800A	3.3V	70/80/100	L, 2K/4K, WPB, SR, EDO	Q4, 94
×16	HY5116160	5V	70/80/100	L, 1K/4K, WPB, 2C/2W	Q3, 94
	HY5116160A	5V	60/70/80	L, 1K/4K, WPB, SR, 2C/2W, EDO	Q4, 94
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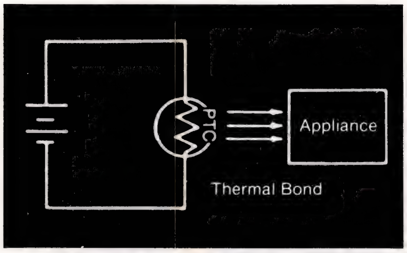

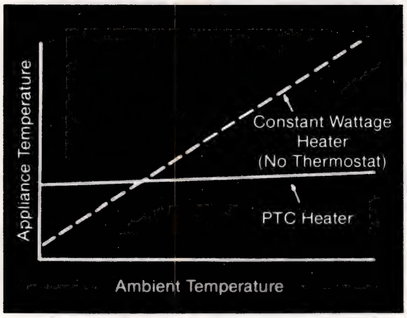

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READER SERVICE 109

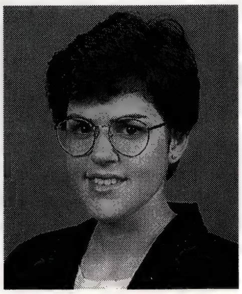
EDA MUST EVOLVE TO KEEP PACE

Simply said, today's design problems can't be solved with yesterday's solutions. Leading-edge system designs—100-MHz pc boards, deep-submicron ASICs, and 40-layer multichip modules—are breaking the backs of existing design tools, methodologies, and processes. For example, a traditional gate-level simulator is quickly overwhelmed by the parasitics in a 1.5-million-gate deep-submicron ASIC. Yet there are engineers who must confront such issues, even though their electronic-design-automation (EDA) environments can't deal with that level of complexity.

While the obvious solution seems to be tool improvements, EDA inadequacy can't always be fixed by enhancing existing tools with more performance, capacity, and features. Sometimes, the solution lies in a brand new tool, an improved methodology, or an updated process.

This issue's cover story, for instance, discusses how Interconnectix Inc., Portland, Ore., embeds a new design approach in a tool aimed at warding off signal-integrity problems in high-speed boards and multichip modules (MCMs) before they happen *(see p. 71)*. Dr. Jonathan Weiss, the company's president and c.e.o., explains that because existing tools just aren't scalable to today's design problems, the company needed to develop its own interconnect-synthesis technology.

Interconnectix realized that current pc-board design methodologies and tools fail engineers working with high-speed designs. The reason is because timing and signal-purity issues don't manifest themselves with those methodologies until the design is expressed in the physical CAD realm. And that's too late. Engineers need to be aware of these problems up front in the design stage. Accommodating that need meant creating interconnect synthesis tools.


LISA MALINIAK
COMPUTER-AIDED ENGINEERING

The same need for a new approach is evident in IC design. A seminar on deep-submicron-IC design, recently given by Epic Design Technology Inc., Santa Clara, Calif., detailed how existing IC methodologies fail for these newest, densest ICs. The existing IC design flow is based on simulation, which often can't handle the IC's size or run fast enough to be practical. But enhancing the current crop of simulators won't work because the computers will always be too slow with too little RAM to do a proper job. In fact, every technology hits a physical limit at some point. "For example," says Simon Napper, vice president of marketing for Epic, "a motorcar won't fly."

Concluding that a new methodology—not new tools—is what's essential, Napper goes on to explain that designing a system on a chip should be approached like system design for pc boards. More specifically, the IC can be thought of as functional blocks from the beginning to the end of the design process. Chips must be defined and partitioned at a high level. Then, the individual blocks can be designed, implemented, and characterized. Finally, static tools can confirm the overall chip performance.

MCM design is yet another technology that pushes the limits of today's EDA software. Harris EDA, Fishers, N.Y., recently launched a new approach to deal with MCM and pc-board design. It introduced a suite of interdisciplinary tools meant to improve design through concurrent-engineering principles. For large design teams, concurrent engineering holds promise for creating a product that's built right from the start. Laurence S. Liebson, president and c.e.o. of Harris EDA, points out that today's tools support a serial, over-the-wall design process. With its new tool suite, however, the company breaks down the walls between the disciplines of logic design, physical layout, and manufacturing.

Interconnectix, Epic Design Technology, and Harris EDA have essentially challenged their industry to accept a new approach to design. Their progress, along with that of others, bears watching.

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Introducing the f
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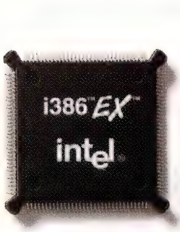

The embedded Intel386™ EX processor.

We asked you what you wanted in an embedded processor, and your suggestions truly hit home. The result is the embedded Intel386™ EX processor. The first and only PC-compatible 386 that's optimized for embedded designs.

The integrated Intel386 EX processor offers power management and low-voltage operation for portable applications. It also increases your design flexibility by allowing you to configure its on-board peripherals according to your own specifications.

For example, the Intel386 EX processor can be programmed to provide DMA-supported serial transfers t reduce the CPU load. Its Chip Select unit eliminates the need for external logic with address decoding, wait-state generation and ready-logic on chip. And its enhanced external bus supports dynamic bus sizing to interface with 8- and 16-bit peripherals.

And designing with an embedded Intel386 processor

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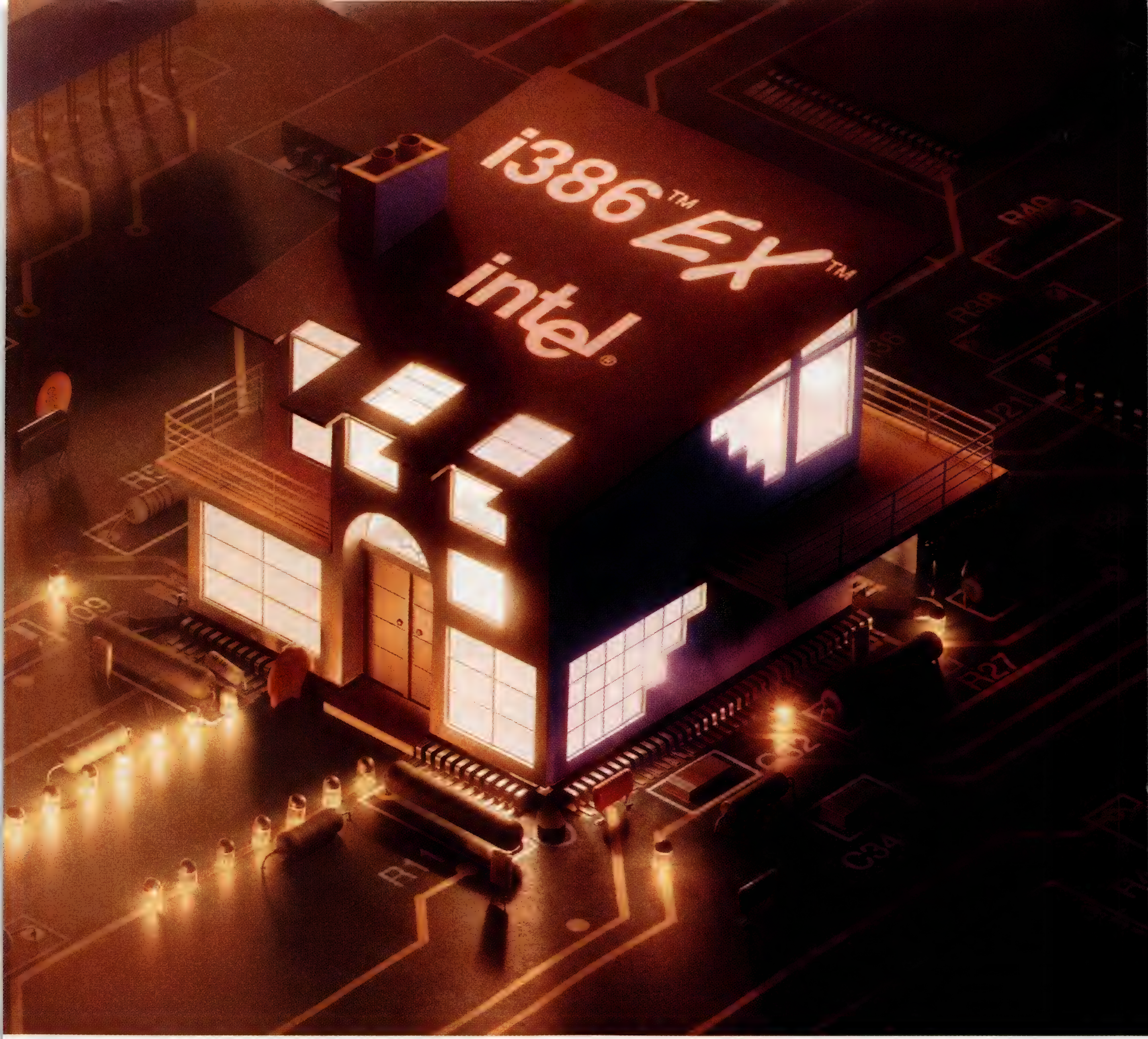


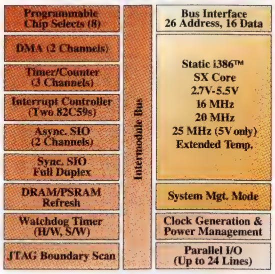
t 386 custom built
d applications.

:ouldn't be easier. The off-the-shelf tools ind support of the PC architecture will illow you to get your designs out more quickly, and differentiate them with familiar nterfaces like DOS and Windows*.

Call us at +44 (0) 793 431155 and equest literature packet USEM01 to get nore information about the embedded ntel386 EX processor. Or contact your listributor to receive Intel386 EX processor samples or to get current pricing of Intel386 SX and DX processors.

Move into an embedded Intel386 EX processor. Because when you want a solution that's optimized for embedded, nobody else is even in the neighborhood.

Embedded Intel386™ EX Processor Block Diagram


Programmable Chip Selects (8)
DMA (2 Channels)
Timer/Counter (3 Channels)
Interrupt Controller (Two 82C59s)
Async. SIO (2 Channels)
Sync. SIO Full Duplex
DRAM/PSRAM Refresh
Watchdog Timer (H/W, S/W)
JTAG Boundary Scan
Intermodule Bus
Bus Interface 26 Address, 16 Data
Static i386™ SX Core
2.7V-5.5V
16 MHz
20 MHz
25 MHz (5V only)
Extended Temp.
System Mgt. Mode
Clock Generation & Power Management
Parallel I/O (Up to 24 Lines)

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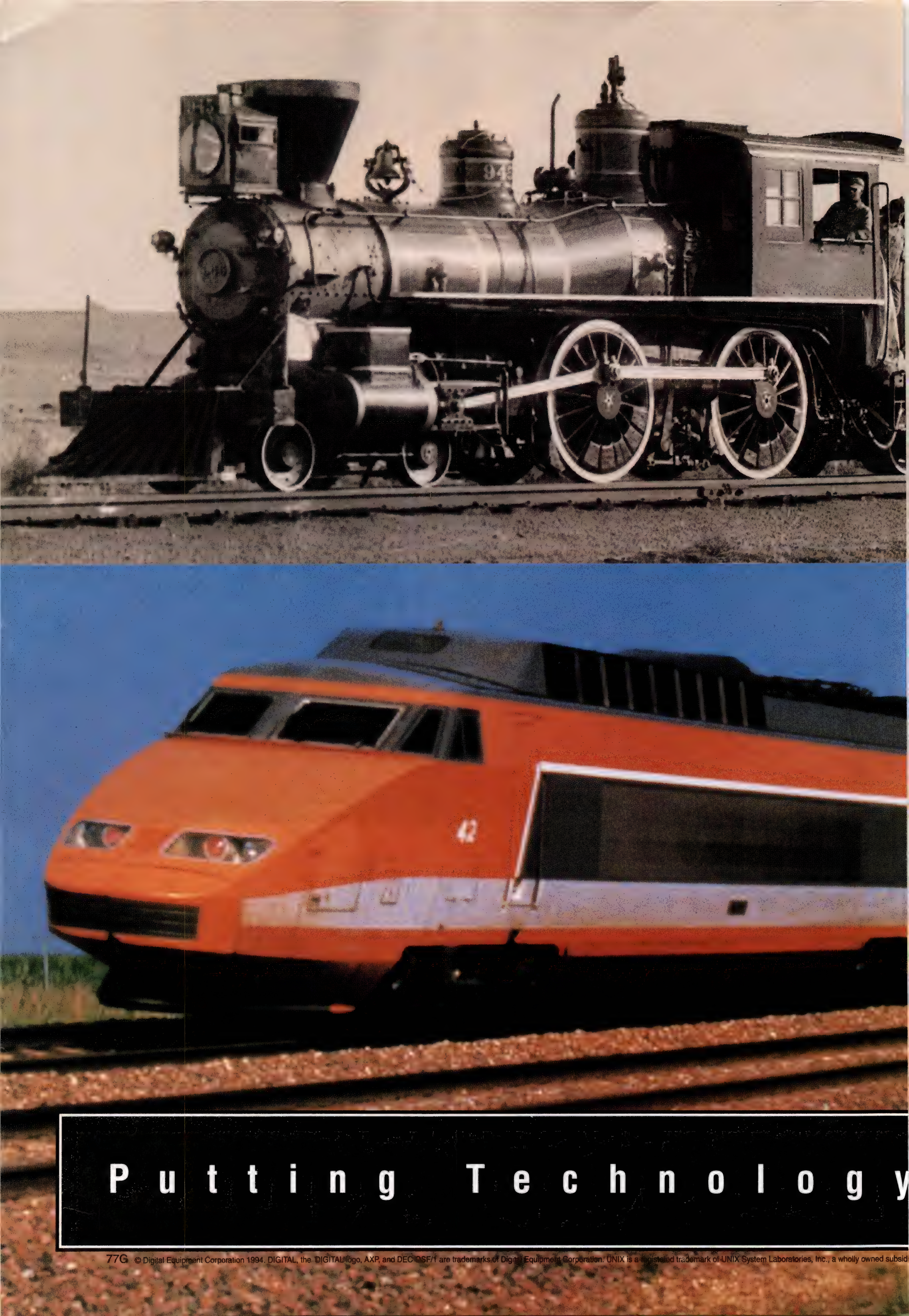

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To Work

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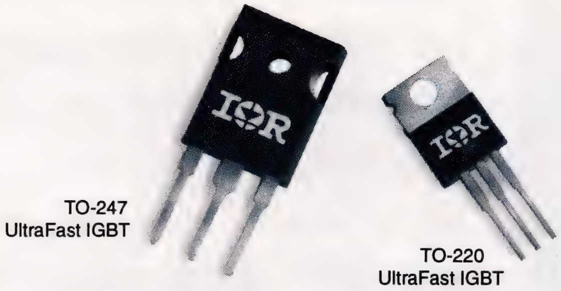
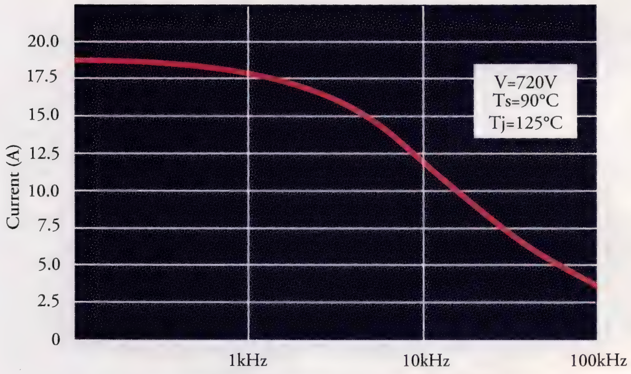
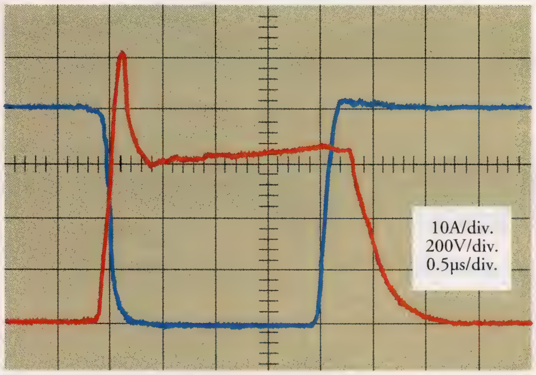
Motor control savings.

Or how to design noise-free inverters that switch faster for less money. The 1200V IGBT *CoPack*.





Output current vs frequency for two IRGPH50U in half-bridge, 50% duty cycle.



Switching waveforms of the IRGPH50U in a clamped inductive load at Tj=90°C.

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TECHNOLOGY NEWSLETTER

JEDEC Devises Tests To Reduce Popcorning

Moisture sensitivity of surface-mounted plastic packages is a major quality and reliability concern for both semiconductor manufacturers and OEMs. The high heat of soldering turns moisture trapped inside a package into rapidly expanding steam—commonly referred to as "popcorning"—that, in the worst cases, causes external cracks. To address this problem, JEDEC developed two test methods. One, test method A112, involves moisture-sensitivity classification, or the maximum floor life or length of time that a package can be exposed to the manufacturing environment without sustaining damage during reflow soldering. Six sensitivity levels range from level 1 (not moisture-sensitive and unlimited floor life) to level 6 (requiring baking immediately before soldering). Verification of long-term reliability is provided by test method A113, which establishes a standard preconditioning flow for plastic surface-mount packages. After undergoing this preconditioning sequence, packages are subjected to a battery of long-term reliability tests involving temperature, humidity, and temperature cycling. For copies of JESD22-A112 and -A113, contact Global Engineering Documents, Englewood, Colo., at (800) 854-7179. *DM*

MCC Has Two-Week MCM Turnaround

A multichip module (MCM) bearing a Sun Viking SuperSparc chip set consisting of a CPU, cache controller, and eight SRAMs was prototyped in just two weeks using a rapid-prototyping process developed at the Microelectronics and Computer Technology Corp., Austin, Texas. The process employs a number of MCC-developed laser and interconnect-routing technologies. A prefabricated substrate, made by MicroModule Systems, Cupertino, Calif., contains most of the interconnections and is customized using a laser process to meet the needs of a given design. MCC's routing software personalizes the interconnections in the substrate based on the description of the chips' pad placement and a net list. The software selects an optimal routing pattern from the thousands of interconnects available in the substrate. Call MCC's Mike Feeley at (512) 338-3282. *DM*

Innovative Models Help With Submicron Design

Several new simulation models developed by AT&T Design Automation, Murray Hill, N.J., offer features geared toward submicron design. For example, the Extended Gummel-Poon (EGP) bipolar-junction-transistor model can be used for analog and digital deep-submicron geometries. The innovative one-piece model is significant because it solves some of the most difficult problems associated with simulating analog designs using submicron devices that have multiple regions of operations. Previous Spice-like models employ different equations for each operating region. This causes convergence and charge-conservation problems due to discontinuities at the boundaries of the regions, resulting in simulation inaccuracies. The EGP offers improved modeling over temperature, accurate high-frequency modeling, and non-ideal behavior modeling of terminal currents that's critical for designs using high-speed ICs. EGP was created for use with AT&T's ATTSIM mixed-signal simulators. Other new models include the company's version of a BSIM3 (a short-channel IGFET model developed by the University of California at Berkeley), and a one-piece ASIM3 MOSFET model that will be released in the future. Because of its one-piece structure, the ASIM3 eliminates glitches found in most MOSFET models at boundaries between operating regions. As a result, it provides more accurate representation of dc current and conductance in all regions. Call AT&T at (800) 875-6590 or fax (908) 582-5145. *LM*

Graphics Engine Trims The Cost Of 3D Images

Designers of PC graphics cards will now be able to handle high-performance OpenGL 3D graphics thanks to the development of a soon-to-be-sampled family of chips called the GLiNT series. The family delivers workstation performance at a price that's attractive for most PC manufacturers. Designed by 3Dlabs Inc. (formerly Du Pont Pixel), San Jose, Calif., the chips will execute the OpenGL calls in the forthcoming releases of Windows NT. Other versions of Microsoft's Windows user interface will use the OpenGL as their standard 3D application-programming interface. Besides selling silicon, 3Dlabs is setting up alliances with board suppliers who can add more value by further customizing the graphics processor. The first alliance was formed with Creative Technology to create a GLiNT variant for multimedia applications by modifying the VHDL-based design model.

With 1 million transistors, the GLiNT 300SX and TX execute 2.5 gigaoperations/s. That's

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lowpass, highpass, bandpass

- less than 1dB insertion loss • greater than 40dB stopband rejection • surface-mount • BNC, Type N, SMA available
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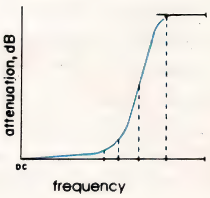
- meets MIL-STD-202 tests • over 100 off-the-shelf models • immediate delivery

LOW PASS



low pass, Plug-in, dc to 1200MHz

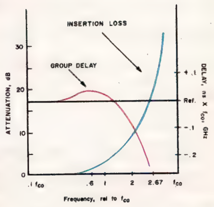
Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200	★LP-250	DC-225	320-400	400-1200
★LP-10.7	DC-11	19-24	24-200	★LP-300	DC-270	410-550	550-1200
★LP-21.4	DC-22	32-41	41-200	★LP-450	DC-400	580-750	750-1800
★LP-30	DC-32	47-61	61-200	★LP-550	DC-520	750-920	920-2000
★LP-50	DC-48	70-90	90-200	★LP-600	DC-680	840-1120	1120-2000
★LP-70	DC-60	90-117	117-300	★LP-750	DC-700	1000-1300	1300-2000
★P-90	DC-81	121-137	167-400	★LP-800	DC-720	1080-1400	1400-2000
★LP-100	DC-98	146-189	189-400	★LP-850	DC-760	1100-1400	1400-2000
★LP-150	DC-140	210-300	300-600	★LP-1000	DC-900	1340-1750	1750-2000
★LP-200	DC-190	290-390	390-800	★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: $11.45

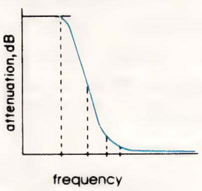


Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco $\overline{X}$	VSWR Freq. Range, DC thru 0.6fco $\overline{X}$	Group Delay Variations, ns Freq. Range, DC thru fco $\overline{X}$	Group Delay Variations, ns Freq. Range, DC thru 2fco $\overline{X}$	Group Delay Variations, ns Freq. Range, DC thru 2.67fco $\overline{X}$
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

HIGH PASS

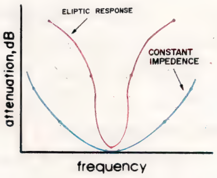


high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1	★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-50	DC-20	20-26	41-200	1.5:1	★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-100	DC-40	40-55	90-400	1.8:1	★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-150	DC-70	70-95	133-600	1.8:1	★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-175	DC-70	70-105	160-800	1.5:1	★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-200	DC-90	90-116	185-800	1.6:1	★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-250	DC-100	100-150	225-1200	1.3:1	★HP-1000	DC-550	550-720	1000-2200	1.9:1
★HP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

BANDPASS



bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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enough to draw 300,000 shaded, Z-buffered, antialiased translucent polygons/s; lines at 750 kvectors/s; and fills at up to 8 million pixels/s. The chips deliver a throughput of 100 million 24-bit Winmarks and accelerate both 2D and 3D graphics. Both chips also include texture-mapping acceleration, with the 300TX offering the highest performance. The SX and TX were designed to be directly interchangeable. A low-end design done with the SX could easily be upgraded to the TX. Furthermore, because the 3D accelerator uses OpenGL, many of the programming tools created by Silicon Graphics, the designer of OpenGL, can be used to speed program development. Contact 3Dlabs' Neal Trevett at (408) 436-3455. *DB*

SEMI SUMMIT LEADS TO GLOBAL COOPERATION

A recent semiconductor consortia summit held in Geneva, Switzerland, hosted by Semiconductor Equipment and Materials International (SEMI), culminated in an agreement by all attendees to cooperate in the study and development of standards and information exchange, and in the coordination of global institute/university research. Primarily dominated by consortia from Europe and the U.S., the summit was aimed at finding ways in which global semiconductor leaders could benefit each other, while still maintaining their individual competitive advantage. As a result, working groups were established to focus on immediate development in the three areas of cooperation. A standards working group will explore and recommend development of standard practices and procedures. Its prime objective will be to obtain a global agreement on the next size of silicon wafers. An information exchange working group will work to identify areas where information exchange can take place to benefit all consortia. In addition, a university/institute research working group will look at various ways to coordinate interaction between universities and industry so that research can be quickly implemented into practical industrial applications. Future follow-up meetings will be held to discuss any findings. The next meeting of the standards working group will coincide with the SEMICON/West Conference and Exhibition in San Francisco, Calif., in July. Contact Chris Greenfield of SEMI/U.S. at (415) 940-6977. *CA*

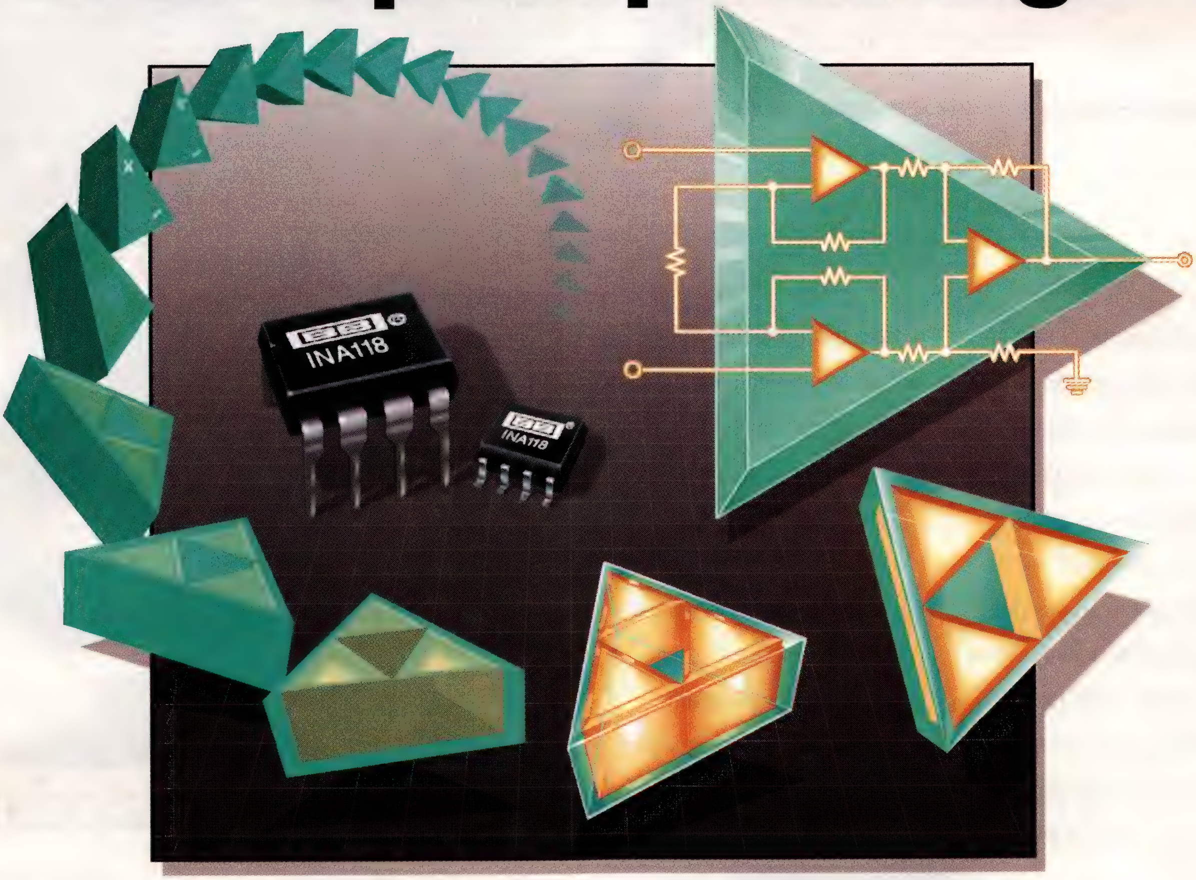
STANDARD FACILITATES DIE-INFO EXCHANGE

The emerging Die Information Exchange (DIE) Format standard promises models and information for bare-die parts in a style that both users and EDA tools can read. DIE Format aims to be the standard method of how to inform engineers of known-good die (KGD) availability, which currently is the biggest limitation in MCM technology. KGD are bare die that were tested and burned-in to achieve the quality of packaged parts. The new standard was developed by the DIE Industry Group, an organization funded by the Advanced Research Projects Agency (ARPA). It includes MCM foundries, EDA vendors, semiconductor companies, and users. Participants include Cadence Design Systems, Harris EDA, IBM, Logic Modeling, National Semiconductor, nCHIP, and Texas Instruments. DIE Format version 1.0 consists of administrative, material, geometric, electrical, thermal, supply, process, and logic-simulation model data. Model information can be generated from an existing database or data sheet, or engineers can create their own DIE-format files if the vendor doesn't supply information in the correct form. A second release of the standard will include timing and test-development information. Although initially focused on digital bare-die technologies, the DIE Industry Group plans to broaden the specification into other technologies, such as analog die and flip-chip. For more information, send an e-mail request to die-info@vhdl.org, or call Logic Modeling's Diane Landers at (503) 531-2252. *LM*

SUPERSCALAR CPU PUSHES SPECINT RATING TO 160

Combining 3.6 million transistors in a superscalar multi-issue architecture has yielded the first samples of the highest-performance PowerPC family member to date—the PowerPC 604. The innovation was produced from a joint design center run by IBM and Motorola, located in Austin, Texas. The 64-bit CMOS chip can issue up to four instructions every clock cycle to six on-chip execution units, thus achieving a throughput of 160 SPECint92 and 165 SPECfp92 when clocked at 100 MHz. The six-stage integer pipeline and three-stage double-precision floating-point unit allow programmers to develop high-performance, graphics-oriented software. Consequently, end users will have moderately priced rendered displays that previously required expensive graphics add-in cards. Multiple on-chip integer units let programmers take full advantage of the chip's computational abilities to handle desktop and server applications. In addition, branch-prediction techniques are used to enhance instruction prefetching as well as speculative execution techniques in order to exploit the improved instruction prefetching and the multiple execution units. The chip, fabricated with a 0.5-μm, 3.3-V CMOS process, includes a phase-locked loop that can multiply the external bus clock by 1, 1.5, 2 or 3X, with a maximum bus clock of 66 MHz. Contact IBM at (914) 642-5449 or Motorola at (512) 891-2839. *DB*

New Instrumentation Amp in an Op Amp Package



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Power Miser

INA118 is a power miser! It operates with power supplies from ±1.35V to ±18V—single-supply down to 2.7V. Quiescent current is only 350μA—it's ideal for battery operated systems and other low power applications. And, internal input protection withstands up to ±40V without damage.

Money Saver

INA118 delivers the highest accuracy and outperforms the competition for a lower price. It's a better solution than any other "make" or "buy" amp out there. You get the best for less.

INA118 Key Specifications

• Low offset voltage	50μV max
• Low offset voltage drift	0.5μV/°C max
• Wide bandwidth	70kHz at G=100
• Low quiescent current	350μA
• Power supply	±1.35V to ±18V
• High common-mode rejection	110dB
• Input overvoltage protection	±40V
• Packages	8-pin plastic DIP, SO-8, dice

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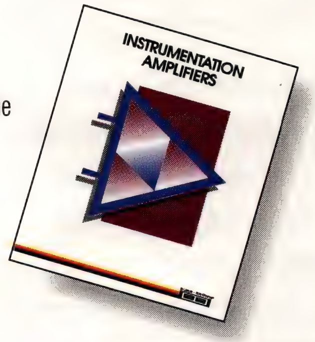

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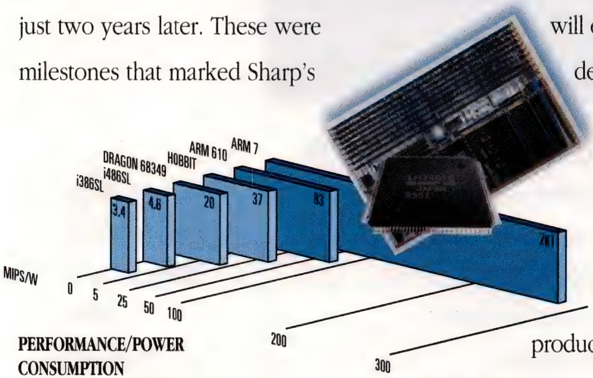

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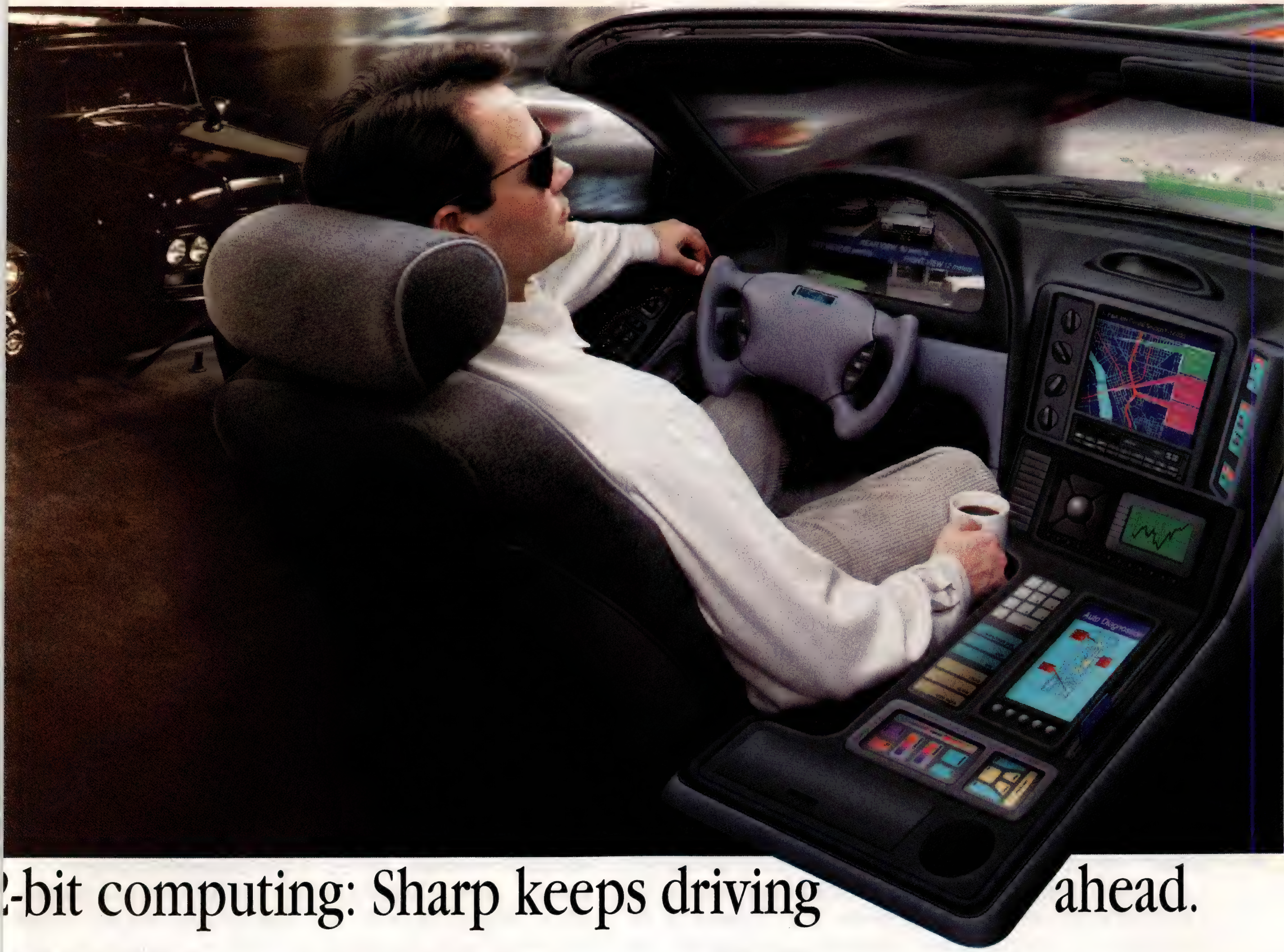

-bit computing: Sharp keeps driving ahead.

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SEC-0594

FABRICATION PROCESS OFFERS INCREASED PERFORMANCE FOR PLANAR FLAT ELECTROLUMINESCENT DISPLAYS

As electroluminescent (EL) flat-panel displays find their way into more applications, the environmental needs put on them continue to intensify. For example, one display might be utilized in an environment with little or no light, while another might be in an environment with extremely bright ambient light. Future displays must not only adjust to these environmental changes, but must do so with little or no degradation in panel quality.

Thanks to the development of a flat-panel display fabrication process known as integral contrast enhancement (ICE), such requirements can now be met by planar EL displays that boast improved contrast and display crispness. The ICE process will be described at the upcoming Society for Information Display (SID) conference, June 12-17, San Jose, Calif.

Conventional EL flat-panel displays consist of three basic layers: column electrodes, EL phosphor, and a reflective row electrode *(see the figure)*. Under typical operation, ambient light enters the front of the display and is reflected back toward the viewer. Light also is emitted from the addressed pixels in the column electrodes, providing light in the direction of the viewer.

Both reflected and emitted light sources have the potential to stray and may themselves be reflected from the metallic electrode. This occurs despite the fact that the primary source of reflected light comes from ambient light.

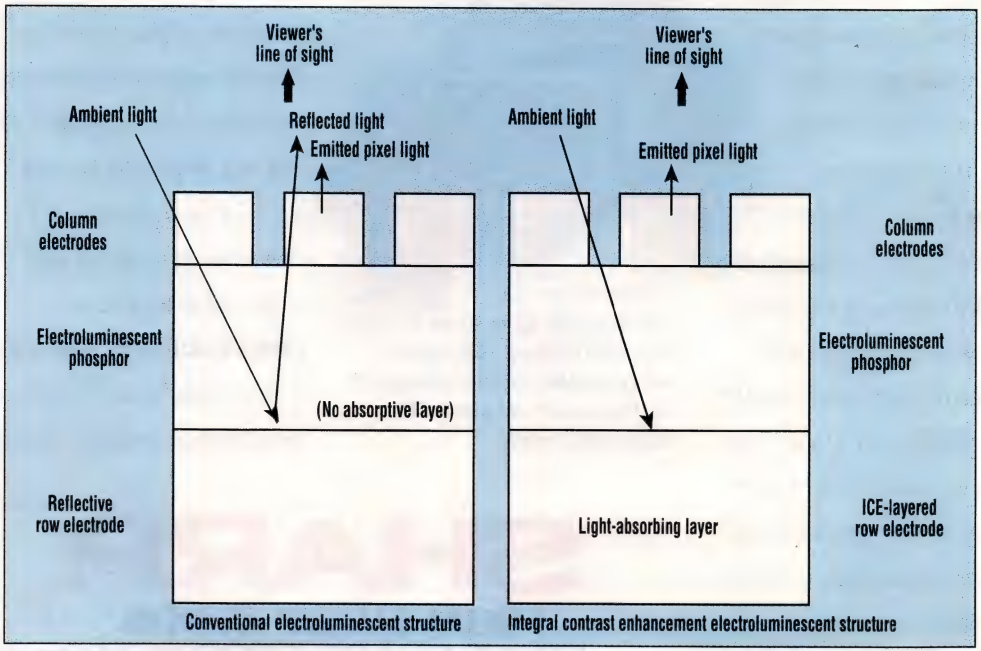
Unfortunately, this stray light, prevalent in conventional EL display structures, makes it difficult if not impossible to achieve high display quality in any type of brightly lit environment. In fact, the brighter the ambient light, the worse the display's overall image quality. This translates into a display with an extremely poor contrast ratio, defined as the ratio of the sum of the emitted and reflected light divided by the reflected light. The higher the reflected light, the lower the contrast ratio. To date, no planar EL display designs exist that can operate in well-lit environments with low contrast ratios yet still maintain good image quality.

Planar Systems Inc., Beaverton, Oregon, solved this problem by developing the ICE process for EL displays. ICE focuses on improving the display contrast ratio of EL displays by allowing stray light to be absorbed, rather than reflected back, at the viewer. This allows for an improved contrast ratio factor of two times greater than that allowed by conventional EL displays in a typical room-lighting environment. In addition, an ICE display maintains excellent contrast performance in ambient-light environments that are brighter by an order of magnitude over normal room conditions. As a result, ICE-processed EL displays can be more easily read and used in a wide range of lighting environments with minimal image-quality degradation.

For the first time, contrast improvement in EL displays is possible without including optical circular polarizing filters. These filters, which go for $25.00 and up, are no longer needed to enhance contrast or improve color uniformity when employing ICE. In fact, when used in a normal light environment, ICE-processed EL displays enjoy a 100% improvement in contrast over a planar EL display with a filter.

An added benefit of ICE-processed EL displays is its enhanced image crispness. Because crispness in a display is determined by how abrupt the transition is from a lit pixel to an unlit adjacent pixel, any significant amount of light scattered to an unlit pixel will cause degradation to an image's crispness. This problem becomes particularly cumbersome as brighter and brighter displays become commonplace. This effect, often referred to as blooming, is prevalent in conventional EL displays. But in ICE-processed EL displays, all blooming effects are eliminated. That's because any light that could potentially leak from a lighted pixel is absorbed in the absorptive layer.

The key to manufacturing an ICE display is the ability to produce an absorptive layer in the EL structure *(see the figure, again)*. This takes place during the layering of the EL thin-film structure, and is deposited between the di-



Conventional electroluminescent structure

Integral contrast enhancement electroluminescent structure

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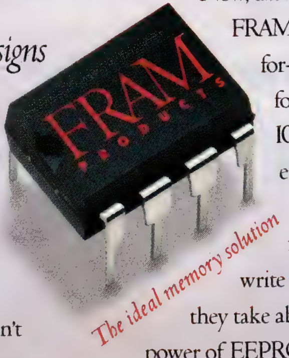

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electric layer and the aluminum row electrode. Because it's an optically-graded index film, the optical characteristics at the surface of the absorptive layer are similar to those of the EL structure. These characteristics change slowly with the grading of the layer to match those of the aluminum electrode. In such a manner, reflections from the metallic electrode structure, which in a conventional display would cause contrast and image crispness degradation, are eradicated.

Although this technology provides a significant increase in image quality and character crispness over conventional EL displays, it's not the final solution to lighting-related problems. Some situations could arise where excessive ambient lighting would cause the image quality to degrade.

Yet, there are many applications where such extreme conditions don't exist. For example, applications ranging from medical and industrial process control to test and measurement are prime candidates for ICE technology. Other applications falling into this category are those in vehicular transportation and telecommunications.

A variety of Planar Systems products fabricated using ICE technology will soon be available. Three of these products will have resolutions of 320 by 256, 640 by 400, and 640 by 480 pixels. Production samples of these models are currently being delivered. Volume production will be available by the year's end.

For more information, contact Planar Systems' Jerry Vieira at (503) 690-1100.

CHERYL AJLUNI

MOLECULAR ENGINEERING AIDS MICROSENSOR DEVELOPMENT

Molecular-level engineering is the driving force behind a novel approach used to build chemical microsensors. Scientists at Los Alamos National Laboratory, Livermore, Calif., successfully modified several different molecules so that one part of the molecule anchors itself directly to a detector, and another part extends as a trap tailored to nab specific types of chemicals.

The sensing molecules bond directly to the surface of the detector that's exposed to the environment. As a result, they form a sturdy, simple device for reliably sensing organic toxins and hazardous materials, while operating under real-world conditions.

The anchor, made up of a silicon-oxygen compound that's called organosilane, bonds directly to materials commonly used in detectors. These materials include the silicon that's used in an electronic chip.

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With this process, the chemistry can sense a contaminant occurrence right at the interface between the detector and the environment. In turn, scientists are able to build in favorable properties to a detector with molecular-level control.

Because organosilane is such an efficient anchor, the Los Alamos researchers allow the molecules to readily assemble themselves into a densely packed monolayer on a detector's surface. The researchers only exposed the surface to a solution carrying the modified molecules and allowed the preferred orientation—the sensing layer that's ready to meet the world—occur through the self-assembly process.

The self-assembly process makes possible the formation of artificial, ordered structures through engineering at the molecular level. By using such a technique, the Los Alamos researchers can form films as thin as a molecule, or they can build thicker films by adding layer upon layer.

Having shown the value of the organosilane anchor for self-assembly and as a durable bond, Los Alamos' researchers are concentrating on modifying the sensing end of molecules to form different bonds. They're particularly excited by the potential of cyclodextrine, a component of starch that can bond with other organic molecules.

Cyclodextrin's molecular structure presents to the world, in essence, a little bucket that fits in external molecules of the right shape. The bucket, in turn, can be tailored to receive specific toxins or contaminants.

When contaminants fill the buckets, their presence changes the thin-film properties on the surface of the detector. These changes, in turn, can be sensed by a variety of techniques.

Sensing techniques include looking for resonating frequency changes in a surface acoustic wave as the thin-film surface gains mass. they also include looking for changes in the suraoptical or electronic properties of the surface.

Because they can bond molecules to different substrates, the researchers have great flexibility in the mode of detection they use. In addition, because the cyclodextrin buckets bind their "guest" molecules, a detector based on this molecule is reversible—it can be used again and again.

The Los Alamos researchers feel that with the design of molecules that can bind specific other molecules, they're building on two decades in chemical recognition. While the researchers have focused their efforts on detecting solvents such as chlorinated hydrocarbons, they feel that the approach they're employing is flexible and could be applied to detecting other organic molecules or metals such as lead, cadmium, or plutonium.

For more information, contact Los Alamos National Laboratory's John Gustafson at (505) 667-7000.

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HARDWARE EMULATION DRAWS SPEED FROM INNOVATIVE 3D PARALLEL PROCESSING BASED ON CUSTOM ICs

When testing complex chip designs, the technique of choice for many electronic engineers is hardware emulation. But traditional hardware emulators, which have worked well as ASIC prototyping tools for final system verification, are too slow to be used in the design phase. However, Arkos Design Inc., Scotts Valley, Calif., believes it has now solved this problem.

Whereas most hardware emulators are based on field-programmable gate arrays (FPGAs), Arkos Design's Pegasus hardware emulator is based on custom ICs. The ICs are joined with a proprietary interconnect scheme.

The Pegasus hardware emulator employs a dedicated architecture based on 3D parallel processing. As a result, it's fast enough to make the emulation process viable as an interactive design and debugging tool.

The hardware emulator is basically a massively parallel logic computer. The computer is made up of arrays of custom multiprocessing ICs, called Hydra chips, that work collectively to emulate complex ASICs

Each Hydra chip emulates a small portion of the target logic by performing a sequence of operations (up to 16) during every target-system clock cycle. As a result, each of the processors, and the interconnection between processors, is used many times within a target-system clock cycle.

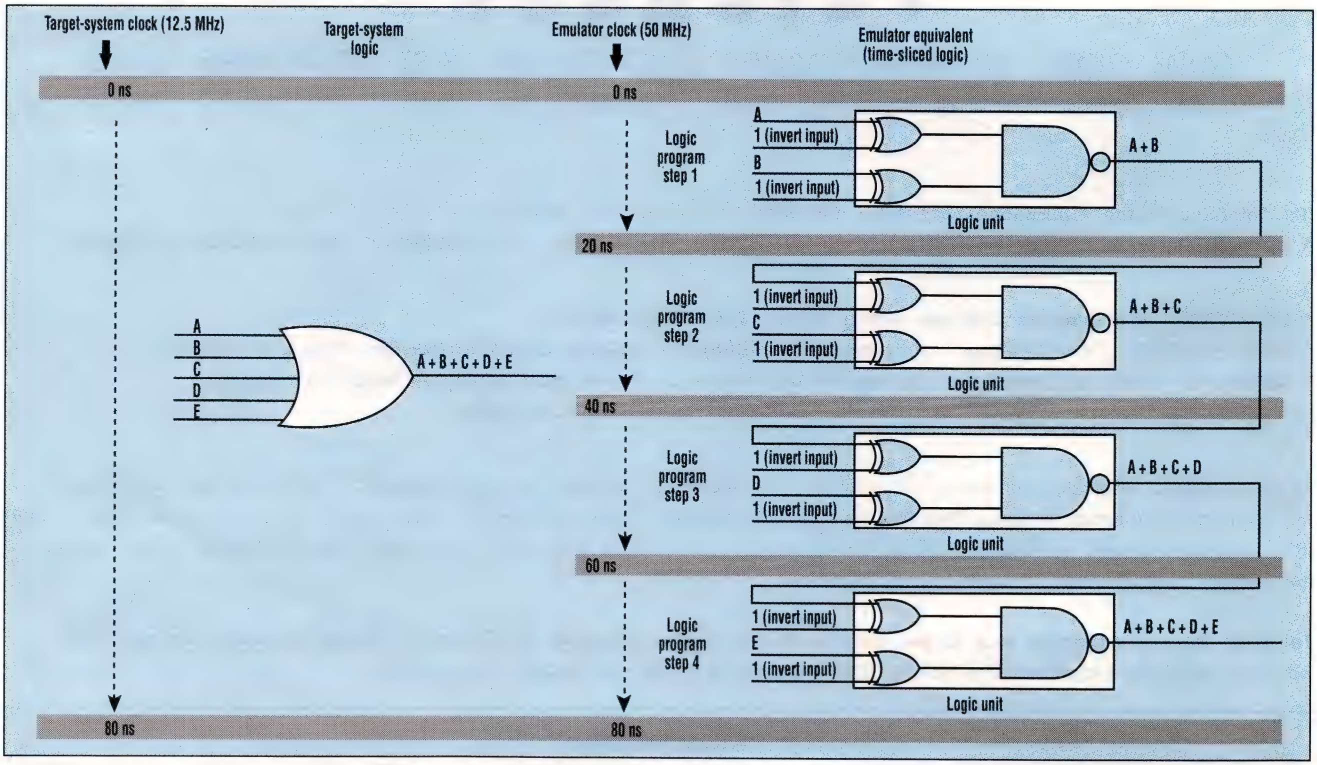
In contrast, FPGA-based emulators assign each target-logic function to a specific element in one of the FPGAs. In addition, each connection between these elements and between FPGAs is dedicated to just one interconnect task.

The difficulties involved in partitioning and mapping a design into a large number of FPGAs demands hours of compilation. What's more, because all of the hardware within the emulator is configured differently after each compilation procedure, engineers must effectively debug the emulator's hardware every time a new net list is downloaded.

This isn't the case with the Pegasus hardware emulator. Its architecture is designed specifically for the emulation of complex logic, and eliminates the need to partition and place-and-route. The system's symmetry, its lack of artificial boundaries, and its extensive routing resources result in fast compilation. There's no translation of the design into the high-level, complex logic blocks of FPGAs. In fact, the only translation is from users' net lists into the corresponding gate configurations of the Pegasus emulator. Only the control software program is changed for each different circuit configuration.

A Pegasus emulator system contains from one to eight boards, each holding 64 Hydra processors. The Hydra chip has 32 logic units that consist of one eight-input NAND gate, inversion circuitry, and a small PLA.

To begin operation, a net list (EDIF or direct) is entered into the Pegasus compiler through a workstation or a Windows-based PC. The compiler converts the net list to Boolean logic equations, much like logic synthesis. It then compiles the equations into a one-



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		x16	60, 70, 80	3Q94/4Q94
Synchronous DRAMs	16 Meg	x8	10, 12, 13	3Q94/4Q94
DRAM Modules	32MB	x32, x64, x72	60, 70	3Q94/4Q94
	16MB	x32, x64, x72	60, 70	3Q94/4Q94
	8MB	x32, x64, x72	60, 70, 80	Now
	4MB	x32	60, 70, 80	Now
88-Pin DRAM Cards and MiniCards	32MB	x32	60, 70	3Q94/4Q94
	16MB	x32	60, 70	3Q94/4Q94
	8MB	x32	70, 80	Now
	4MB	x32	70, 80	Now
SRAMs	4 Meg	x4, x8, x16	12, 15, 20, 25	3Q94/4Q94
	1Meg (revolutionary)	x4, x8, x16	15, 20, 25	Now/3Q94
	1Meg (evolutionary)	x1, x4, x8	15, 20, 25	Now
	256K	x1, x4, x8	12, 15, 20, 25	Now
Synchronous SRAMs	1 Meg	x18, x36	7, 10, 12, 15, 17	Now/3Q94
SRAM Modules	4MB	x32	15, 20, 25	4Q94/1Q95
	1MB	x32	20, 25	3Q94/4Q94
	512KB	x32	20, 25	3Q94/4Q94
	256KB	x32	15, 20, 25	Now
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million-bit-wide machine-language logic program that's downloaded through a SCSI interface into the emulator's SRAM for use by the logic processors. During the emulation process, the software program tells the Pegasus system what each logic unit should do in each time step to implement the ASIC prototype.

The logic programs execute within one target clock cycle, and implement the target logic in steps. Because the emulator runs the program faster than the target clock, the program can be up to 16 words long. Each logic unit then has up to 16 cycles, or steps, in which to perform operations and get data on or off the unit. This greatly expands the routing options.

The Pegasus emulator runs at a clock frequency of up to 50 MHz, and, consequently, emulates systems at approximately 3 to 12 MHz. Users can opt to reduce the number of steps in the emulation to increase its operating speed.

Target logic can contain synchronous and asynchronous clock signals. For synchronous operation, logic that requires 16 cycles to complete can have a maximum target clock running at 3.1 MHz (50/16 = 3.1). But if the logic finishes in eight cycles, the maximum target clock runs at 6.2 MHz (50/8 = 6.2).

Consider the implementation of a 12.5-MHz five-input OR gate *(see the figure)*. First, the OR operation of the five signals (A + B + C + D + E) is translated into four one-word, machine-language programs, each 1 Mbit wide, that are stored in a logic unit's SRAM. Because the logic programs are read directly into RAM, there's no logic-partitioning problems. In addition, compilation is fast and requires no user intervention. During the emulation, the logic unit executes the first logic program (A + B); the second (A + B + C); the third (A + B + C + D); and finally the fourth (A + B + C + D + E). Because there are four steps, the Pegasus 50-MHz operating speed results in a prototype operating speed of 12.5 MHz (50/4 = 12.5).

There are many benefits to the system's architecture. Pegasus models the target designs only in software, so no new clock skew or propagation delay problems are introduced. And because the actual hardware of Pegasus never changes, users don't need to debug the emulator. Users need only debug their target logic. The FPGA-based emulators reconfigure circuitry, which can cause timing problems. In the Pegasus logic processors, like a microprocessor, only the control program changes.

A Pegasus box, which can sit on the desktop, houses up to eight boards. Each board holds 64 Hydra ICs, 4 Mbits of SRAM for memory emulation, 2 Mbytes of trace RAM for logic analysis, and an extensive 3D interconnect. There are X- and Y-axis connections between adjacent chips on one board, and Z-axis connections between chips on neighboring boards.

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A Hydra chip is a 500,000-transistor full-custom IC built on a 0.8-µm CMOS process and housed in a 100-pin plastic QFP. Each chip holds 32 logic units as well as 30 kbits of program RAM.

Boards populated with Hydras can emulate 30,000 gates of logic and 4 Mbits of RAM. As a result, a fully-populated Pegasus system has eight boards capable of emulating 240,000 gates of logic, in addition to 32 Mbits of high-speed SRAM. Emulation memory is composed of high-speed 12-ns static RAM, and can model numerous types of memory structures. The individual memories are able to be combined in width or depth. Contents can be viewed and written at each breakpoint.

The built-in logic analyzer has a patented trace methodology. Every node in the net list is accessible and viewable on-screen. Hardware connections or even pre-definition of nodes aren't needed. The 32-kbyte trace RAM on each Hydra chip continually downloads the processor's internal state to create a mirror image for analysis. The system can do this for 32,000 time slots.

The Pegasus hardware emulator is available in either 25-, 50-, 100-, or 200-kgate configurations. Pricing ranges from $36,300 to $115,000.

For more information on the Pegasus hardware emulator, call Arkos Design at (408) 461-8100, or fax at (408) 438-5819.

LISA MALINIAK

MULTIPROCESSING VERILOG SIMULATOR EXPLOITS THE PARALLEL NATURE OF HDLS

Often, parallel processing is used to wring more speed from software applications. Of those applications, logic simulation—which is essentially discrete-event-driven software—is particularly difficult to parallelize. Now, however, one firm, Chronologic Simulation, Los Altos, Calif., has come up with a multiprocessing Verilog simulation environment that eliminates the problems associated with parallelism.

The scheme exploits the parallelism usually found in hardware description languages (HDLs) to deliver significant speed gains. This new multithreaded version of Chronologic's Verilog Compiled Simulator (VCS) runs on Sun Microsystems' Sparc-based shared-memory multiprocessing (SMP) workstations.

Actually, hardware itself is inherently parallel because gates, macrocells, ICs, and pc boards are separate processing units operating simultaneously with each other. An HDL has constructs that represent the parallel nature of hardware—modules used to define logical functions ranging from gates to complete systems. But the fundamental problem in perform-

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ing parallel simulation using HDLs is the synchronization of interconnection between modules.

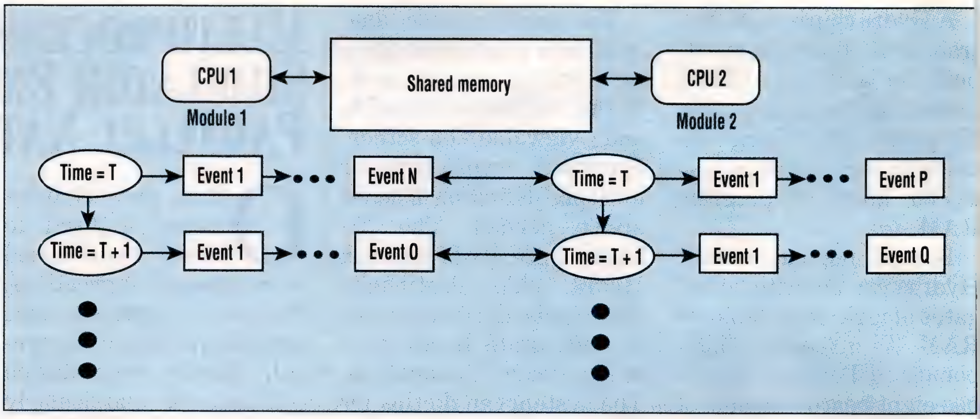
With VCS/MT, each module simulates independently within a thread on an assigned processor *0 (see the figure)*. Threads have their own event queues that schedule events at each time tick. Schedulers move to the next time tick only when all other queues also can proceed.

All of the processors tap into a central shared memory. The software runs on Sun Microsystems' Sparc 10 and Sparc 20 workstations, which can be expanded to four CPUs, and the Sparc Center 1000, which is expandable to eight CPUs. Each thread has its own mailbox in the shared memory. Mailboxes can be accessed by other threads as needed.

VCS/MT handles all communication between modules that span processors. This approach, made possible by the tight coupling of the independent processors in the Sparc SMP system, avoids many of the synchronization problems of previous parallel techniques. Processing time is reduced because there's no need to back up in time and rerun simulations.

Changes made to the existing single-processor VCS software to adapt it to multiprocessing are transparent to users. Basically, Chronologic altered the data structure so that information sharing occurs across multiple CPUs, and one CPU recognizes when data is being used by another.

Because VCS/MT is based on a proven simulator, users don't have to modify their designs significantly to exploit the parallel capabilities of the system. Within an existing Verilog model, users mark modules that are relatively independent and can run on separate processors. One file associated with the model designates the path names of modules, and indicates how they can be distributed. From here, VCS manages the simulation across processors in the SMP system.



An engineer working with a CPU design, for example, might allocate the integer unit, floating-point unit, memory-management system, and cache controller to separate threads on four different processors. VCS/MT then takes care of distributing and managing the modules across processors in the SMP system.

Performance improvements over standard VCS vary, depending on the simulated system. Preliminary results indicate that parallel simulation will work well for circuits with a small amount of activity across parallel partitions, a balanced amount of computation across parallel partitions, and a large amount of activity at each point of simulated time.

For more information, call Chronologic at (415) 965-3312, or fax them at (415) 965-2705.

LISA MALINIAK

FABRICATION AND CIRCUIT ADVANCES PROMISE 0.10-μM PROCESSES, GIGABIT DRAMS, AND TOP-PERFORMING LOGIC

Gigabit DRAMs and 1000-MIPS processors may well be here within a few years. That's the message coming out of the Symposium on VLSI Technology (June 6-9) and the Symposium on VLSI Circuits (June 9-11), both of which detail advances in IC-processing and device technologies.

The Symposium on VLSI Technology, which has an accompanying workshop on "Limits of Device Scaling", June 6, focuses on advances in processing—lithography, metallization, oxide growth, deep submicron CMOS, and biCMOS structures. The Symposium on VLSI Circuits provides details of circuit implementations that will herald next-generation memory ICs, microprocessor devices, and other ICs.

At the VLSI Technology conference, IBM scientists, Yorktown Heights, N.Y., will discuss an implementation of a 0.1-μm CMOS process. Design trade-offs between gate delay, active power, and standby power when operating the circuits at supply levels of 0.5 V are examined. They've obtained experimental results that show ring-oscillator delays of 100 ps and a power-delay product of just 0.03 fJ/stage (switching factor = 0.01) with a 0.4-V supply. That represents a 20-fold reduction in power for the same delay speed compared with a 0.25-μm CMOS process.

As devices shrink and voltages drop, the threshold-voltage variation from device to device becomes more critical in the fabrication process. Researchers at Motorola Inc., Austin, Texas, examine the effect of V_T variations due to random doping fluctuations on the stability of SRAM cells and on CMOS logic performance. In their modeling, they estimate that the largest V_T mismatches on a typical SRAM chip might increase from about 100 mV (for a 0.35-μm, 16-Mbit SRAM to 175 mV for a 0.1-μm, 4-Gbit SRAM. On logic devices, a variation of about 30% in the drain saturation current of the transistors

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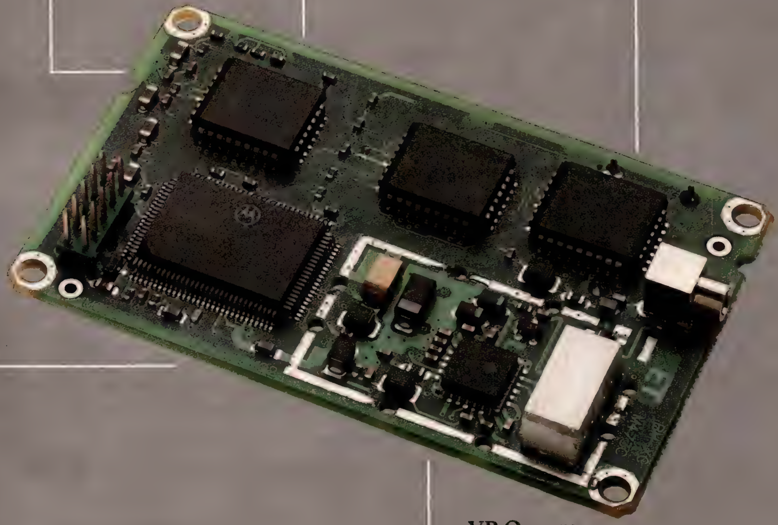

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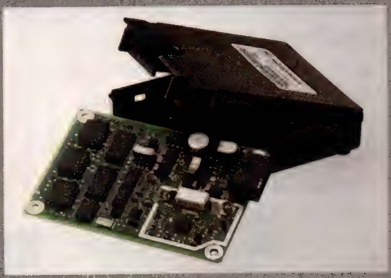

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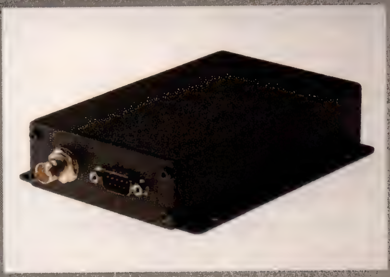

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could be expected on a circuit with 1 billion 0.1-µm devices operating with a supply voltage of 1.5 V.

For gigabit DRAMs to become reality, new capacitor structures and materials are needed to ensure that storage cells can hold a sufficient charge as the cell area shrinks. To that end, lead-zirconate-titanate (PZT) films doped with lanthanum are described in a joint presentation by the Advanced Products Research and Development Laboratory (APRDL) of Motorola, and the University of Austin's Microelectronics Research Center. Using a 5%-doped PZT film for the capacitor's dielectric, a charge-storage density of 100 $fC/\mu m^2$ with a $V_{DD}/2$ of 1 V was achieved.

Thin films of barium strontium titanium oxide (BaSrTiO) are the subjects of discussion from scientists working jointly at the Matsushita Electronics Corp., Osaka, Japan; the Symetrix Corp., Colorado Springs, Colo.; and the Microelectronics Research Lab at the University of Colorado at Colorado Springs. Such films have high dielectric constants. Capacitors made with ultra-thin BaSrTiO films achieved a unit capacitance of 95 $fF/\mu m^2$ with an applied voltage of 2 V. And, researchers at the University of Austin's Microelectronics Research Center also are looking into the fabrication of ultra-thin (30 A) oxide-nitride storage-capacitor dielectrics.

Besides the strong focus on digital technologies, the presentations take a look at various mixed-signal processes that achieve high operating speeds at low power levels. For instance, researchers at AT&T Bell Laboratories, in Holmdel, N.J., and AT&T Microelectronics, in Allentown, Pa., jointly describe a mixed-signal low-power biCMOS process that can yield 6-GHz phase-locked loops that operate from just 2 V and consume a mere 60 mW. Those results were achieved by using a shallow arsenic buried layer, combined with a fully-recessed, locally-oxidized isolation scheme.

Although developed initially for high-performance biCMOS SRAMs, a low-RF-noise but high-performance bipolar transistor created by Motorola's APRDL and several other Motorola research divisions also delivers excellent small-signal RF performance. Fabricated with 0.35-µm features, the transistors were used to produce current-mode-logic gates that operate at supply levels of only 1 V and have a power-delay product of 4.8 fJ.

At Texas Instruments' research labs in Dallas and Saitima, Japan, researchers came up with a 30-V extended-drain structure that forms high-voltage CMOS and lateral DMOS devices for both high-side and low-side driver applications. With a simple twin-well, single-tank, one-level-metal process implemented with 2-µm features, on-resistances of 0.49 $m\Omega\text{-}cm^2$ for n-channel devices and 1.9 $m\Omega\text{-}cm^2$ for p-channel transistors were realized.

WANT TO GO?

Pre-registration for the Symposia on VLSI Technology and Circuits, and the June 6 workshop, can be done through Widerkehr and Associates, 1545 18th Street NW, Washington, DC 20036; phone (202) 986-1137, fax: (202) 906-1139.

At the VLSI Circuits Symposium, presentations will examine analog as well as digital technologies. For instance, a 900-MHz CMOS RF power amplifier that achieves a 30% conversion efficiency at 3 V will be described by researchers from the Integrated Circuits and Systems Laboratory at the University of California at Los Angeles.

In addition, a full-function, 1.5-GHz, direct-conversion transceiver IC targeted at mobile communications will be described by Siemens AG and Phoenix VLSI Consultants Ltd., Towcester, England. The chip, produced using a 0.8-µm bipolar process, contains all of the RF functions for a transceiver except for the antenna. Such a circuit could make possible a two-chip handheld communicator.

Video-speed analog-to-digital and digital-to-analog converters (ADCs and DACs) also are key circuits, because they help lower the complexity and cost of filmless digital cameras as well as multimedia and videoconferencing systems. A 1.5-V, 20-MHz, 8-bit ADC will be the focus of a presentation by NEC Corp., Tokyo, Japan. The converter employs a hierarchical tree structure based on current mirrors. Going NEC one better, Toshiba Corp., Kawasaki, Japan, will describe a 10-bit, 20-Msample/s ADC that runs at 3 V and includes self-calibration to correct gain errors and the settling time of the subrange amplifiers. It consumes just 24 mW. With a 1-V p-p input and a 3-V supply, the chip delivers 10 bits with a ±0.4-LSB differential nonlinearity.

Designers at Harris Semiconductor, Palm Bay, Fla., along with the University of Illinois, Urbana, built a 13-bit, 10-MHz ADC with a background calibration scheme. They developed real-time, digital-domain code-error calibration that focuses on improving converter nonlinearity in real time while the ADC is operating, instead of just prior to a conversion. The technique uses an oversampled delta-sigma ratio calibrator that works in the background, synchronously, with the converter.

By employing digital self-compensation on a 10-bit CMOS DAC, Samsung Electronics Co., Bucheon, Korea, and Seoul National University, Seoul, Korea, were able to compensate for errors without interrupting DAC operation. The scheme isolates the compensation procedure from the high-speed operation of the current switch, decreasing the nonlinearity of a 10-bit DAC to 0.22 of an LSB, versus 0.47 LSB without the scheme.

On the digital side, a number of papers look at the future of flash-memory technologies. An 18-Mbit serial flash memory, jointly developed by researchers at SunDisk Corp., Santa Clara, Calif., and Matsushita Electronics Corp., Kyoto, Japan, will show the use of 0.5-µm design rules and circuit compaction techniques that keep the chip area to just 74 mm^2.

Concerning high-speed programming and program-verify schemes for low-voltage flash memories, researchers at Hitachi Ltd., Tokyo, Japan, will detail three schemes to speed up programming and program verification. One approach fixes the p-well bias for row subdecoders, allowing the program-verify stage to follow the program stage without an additional well-charging operation. Next, by using an internal

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program-end detection circuit, the completion of the program mode can be checked in one cycle, freeing the external CPU from the memory chips. Finally, a scheme employing variable-pulse widths for programming helps cut the total number of verifications.

Designers at Mitsubishi Electric Corp., Itami, Japan, will detail studies to detect overerasure, which will help extend the lifetime of flash-type memories as well as allow low-voltage operation. By detecting and minimizing the overerasure, it's expected that the threshold voltage distribution can be tightened across a chip, permitting a lower programming voltage to be used.

A novel charge-pump structure developed by Toshiba Corp., Kawasaki, Japan, also will be unveiled. The charge-pump scheme, employed in a NAND-cell flash EEPROM, is able to change the number of stages and the capacitance of the charge pump (which are conventionally fixed values) as the output voltage is boosted. That helps reduce the voltage rise time by about 50% over the conventional scheme without increasing average current levels.

Furthermore, Toshiba's unique NAND memory cell in its flash memories is being examined for use in a DRAM. In that presentation by Toshiba, researchers describe a memory architecture using a cascaded arrangement of DRAM cells to form the NAND-structured DRAM. However, in their first attempt, they observed an array noise problem due to the open bit-line arrangement they had selected. In a second version they will describe, a new cell arrangement suppresses the noise by 40% and reduces the chip area by 37% (versus a conventional DRAM with a folded-bit-line architecture).

Trimming the active power of logic circuits is always a big challenge. As switching speeds are driven ever faster, more attention must be paid to trimming the internal power of complex logic chips. One scheme developed by Hitachi employs an internal bus architecture with a data-dependent logic swing. The scheme reduces the dynamic power to 1/16th that of a conventional bus (for a 16-bit-wide bus). The approach uses a dual-reference sense-amplifying receiver that converts a reduced-swing bus to a CMOS-level signal without any loss of noise margin or speed. In another presentation, Hitachi will describe a half-swing clocking scheme that promises to save 75% of the power now consumed in clocking circuits.

Additional papers focusing on low-power schemes include a multiplexer-based architecture for high-density gate arrays from TI, and an Adiabatic computing architecture that employs a novel 2N-2N2D logic family developed by AT&T Bell Laboratories. The AT&T logic scheme dissipates about one-third of the energy that conventional CMOS logic consumes per computation. Most of the energy needed for turning transistors on and off is recovered and returned to the power supply. Some analysis results on recovered-energy logic also will be presented by the Laboratory for Electromagnetic and Electronic Systems at the Massachusetts Institute of Technology, Cambridge.

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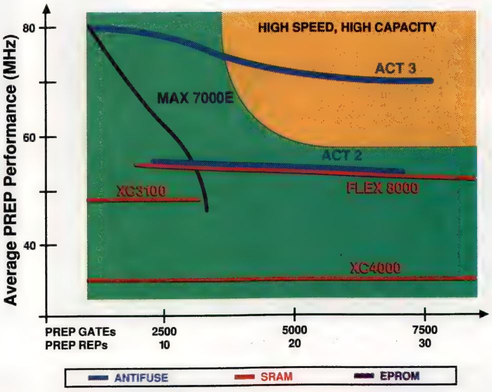

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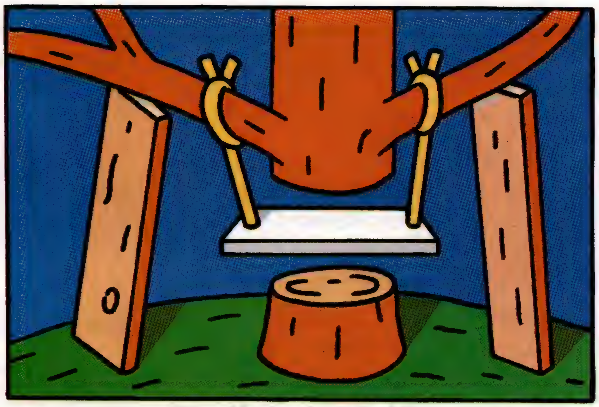

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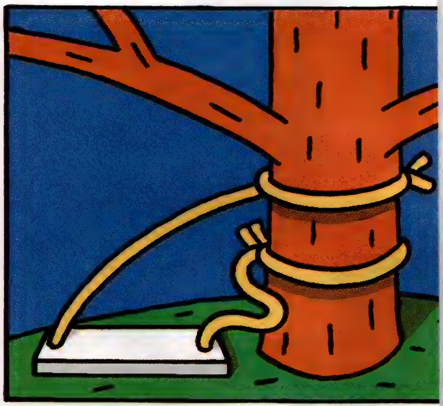

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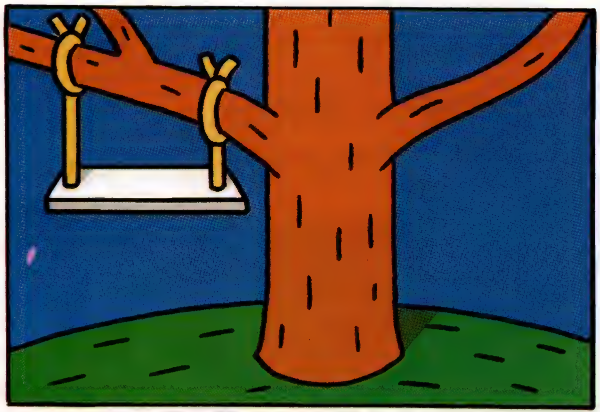

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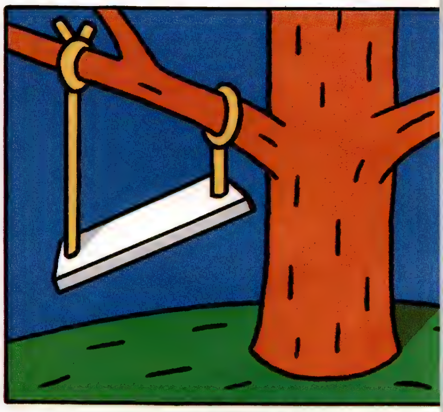

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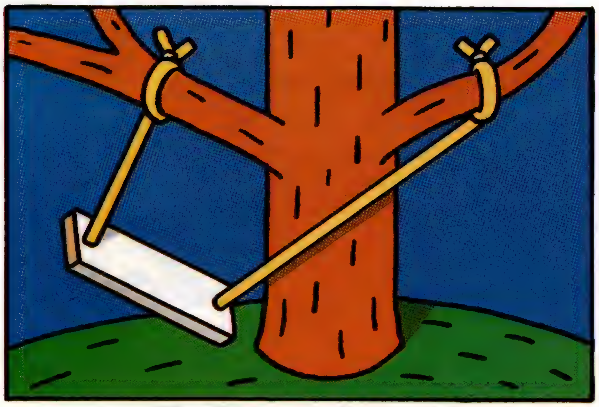

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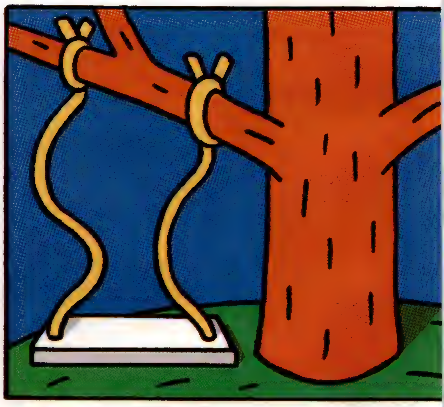

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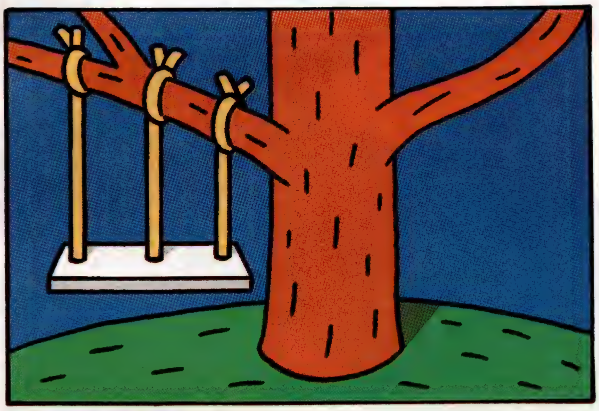

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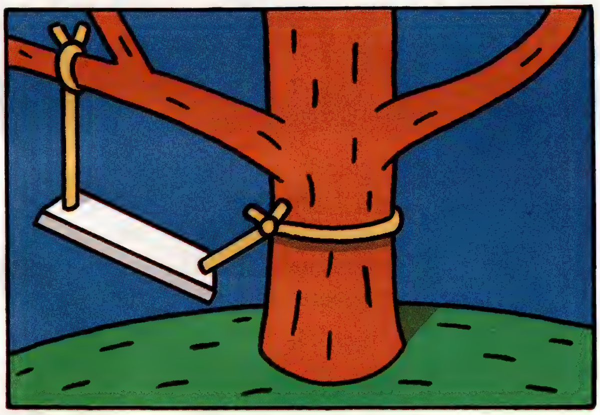

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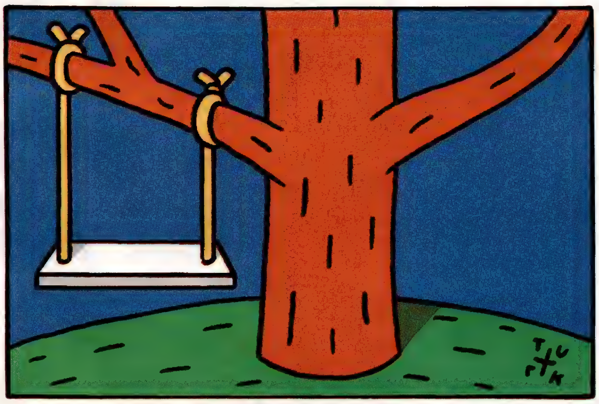

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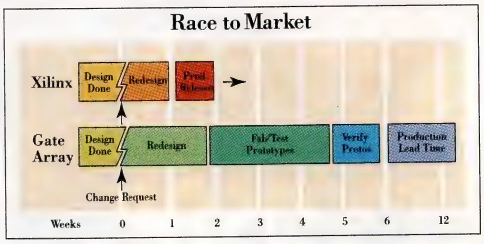

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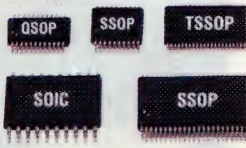

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TECHNICAL PAPERS AND PRODUCTS REFLECT THE TREND TOWARD RAISING THE LEVEL OF DESIGN ABSTRACTION.

LISA MALINIAK

Engineers eager to curtail the rapidly increasing size and complexity of today's ICs and systems are looking to raise the level at which they design. By raising design abstraction, engineers essentially can start at a higher level that requires fewer implementation details. At this year's Design Automation Conference, taking place June 6-10 in San Diego, Calif., the trend toward high-level design is one of the common threads running through DAC's technical papers, tutorials, and over 110 vendor exhibits.

Two high-level tools in particular will share the DAC spotlight—electronic system design automation (ESDA) and synthesis. ESDA tools are key to defining a system and managing the design flow at a high level. Synthesis software automates the transition between abstraction levels, and is essential to the productivity gains promised by high-level design. Over one-quarter

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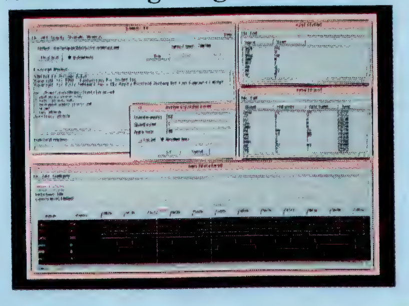
EPS' technology uses compaction and circuit abstraction while maintaining high memory efficiency. Both simulators take full advantage of today's RISC architectures by making extensive use of cache memory and the processor's pipeline. Memory efficiency is achieved through compact data structures and a small simulation kernel. In fact, designs with as many as one million primitives can be simulated with 64 Mbytes of memory.

The LX2 and FX2 tools retain the interactive and debugging capabilities of the company's previous products. Users can input a wide variety of standard net-list formats and libraries, including EDIF and Verilog.

VCX2 is a software tool that allows a Verilog design to be simulated by the Simetri tools. It includes support for Verilog programming-logic-interface routines, the SDF file format for back-annotation of delays, and Verilog hardware-description-language constructs. VCX2 also includes a syntax checker and a net-list flattener, and is compliant with the Open Verilog International Version 2.0 specification. It's targeted at current Verilog users doing ASIC and full-custom IC design who need higher performance and memory efficiency.



The Simetri-LX2 logic simulator, Simetri-FX2 fault simulator, and VCX2 Verilog tool run on Unix workstations. All three will ship in the third quarter. Call the company for pricing and additional product information.

Evaluations Per Second Inc.,
1601 Trapelo Rd., Waltham, MA 02154; (617) 487-9959.

CIRCLE 601

■ *Booth 916*

of the 44 technical sessions cover topics related to system-level design or synthesis technology. Moreover, the keynote address will be delivered by Doug Fairbairn, president and c.e.o. of Redwood Design Automation, San Jose, Calif. Redwood offered some of the first commercial ESDA tools.

Because ESDA has many applications, numerous description levels, and a host of parameters to consider, it can't be limited to a specific definition or set of parts. Instead, ESDA suggests a level of design where engineers can consider the entirety of what they must deliver to end users. That may include electronic hardware, software, sensors, electromechanical parts, and whatever else comprises a product.

The DAC offers a glimpse into the portion of ESDA aimed at defining system components destined for hardware and software. Two general areas of research can be gleaned from the papers and topics presented: how to fully describe an electronic product, and how to most efficiently realize the description in an implementation.

MODELING INTERCONNECT

System design typically focuses on complete, discrete entities. These entities are made up of many components (hardware and software), and can be modeled en masse with ESDA tools.

Today, many products consist of systems communicating and cooperating with other systems. ESDA techniques have worked well to define specific system blocks, but not the I/O interchange among them. The tools must address these I/O interfaces so that engineers can integrate system components which often use incompatible protocols to communicate with each other.

Most current asynchronous design tools focus on creating one interface circuit. However, engineers must design interacting modules

SIMULATION ACCELERATOR RUNS AT TWICE THE SPEED OF SOFTWARE

The Paradigm XP Super Fault hardware accelerator developed by Zycad delivers 20 to 120 times the speed of the fastest fault-simulation software running on a powerful workstation. This product is the latest addition to the company's Paradigm Verification workbench—a tool suite for concurrent verification of complex ASICs and systems.

Zycad also is announcing a set of features that lets users more efficiently perform fault simulations on large systems, even if they include full or partial internal scan. The new features are: an interactive fault tracer, test-directed fault simulation, strobe windows, and parallel loading of scan vectors.

In addition, the Paradigm XP Super Fault simulator supports concurrent simulation using accurate pin-to-pin timing, which is an important feature for the 50% of designs that contain asynchronous elements. The system provides capacity from 64,000 to 4 million gates for fault simulation, and from 256,000 to 16 million gates for logic simulation. Pricing starts at $79,000.

***Zycad Corp.,** 47100 Bayside Pkwy., Fremont, CA 94538-9942; (800) 243-7286 or (510) 623-4400.* CIRCLE 602

■ *Booth 400*

TOOLKIT HELPS CREATE EDIF 3 0 0 TRANSLATORS

Easy translation of design data into the Electronic Design Interchange Format (EDIF) 3 0 0 is critical to that standard's widespread adoption. The DXE300 EDIF toolkit is intended to provide a productivity boost in the development of EDIF solutions.

The toolkit, which the company calls an EDIF-translator development environment, provides all of the software modules and support libraries, as well as the intermediate format, required for any EDIF-translator development project. It supplies a predefined pathway into and out of EDIF 3 0 0, bringing open-system capabilities to a wide range of design-automation tools and systems.

Advanced features of the toolkit include the elimination of time-consuming scans of databases and files, and elimination of all EDIF-dependent data-sequencing requirements. It also provides command-line argument support and other useful functions. A procedural interface to the toolkit's own persistent intermediate database allows users to import and export data in any order. There's also a full suite of EDIF utilities to ensure the correctness of the final translator product.

By using the DXE300 toolkit, the success of translator-development projects is no longer threatened by the complexities of EDIF. The toolkit is useful to EDA vendors who require an EDIF 3 0 0 interface for their tools, and for end users who want to integrate their own design environments.

Pricing for the DXE300 EDIF-translator development environment starts at $5000. The system contains the EDIF 3 0 0 reader, EDIF 3 0 0 writer, and database and procedural interfaces. Many other options are also available.

***Engineering DataXpress Inc.,** 5 Town and Country Village, Suite 736, San Jose, CA 95128-2026; (408) 243-8786.* CIRCLE 603

■ *Booth 1911*

that communicate with each other in potentially complex and intricate ways. Even if each individual module can be synthesized correctly, the composition of communicating modules may not work properly. Engineers need ways to model how the interface modules communicate with each other, so they can verify that module cooperation is consistent.

A paper in Session 6 titled "A Communicating Event-Based Model for Specification and Synthesis of System Interfaces" describes communicating interface processors (CIPs), which are models for system interfaces. The authors, from IMEC in Leuven, Belgium, based this model on labeled versions of the commonly employed Petri nets. Each interface component is expressed as a labeled Petri net using an abstract synchronization method based on a type of semantics called rendezvous.

With this approach, engineers can specify multiple levels of communication among high-level blocks, from high-level abstractions to actual signal transitions. The authors also defined a new algebra for communicating Petri nets that allows engineers to manipulate communicating interface modules and verify their consistency. In addition, the modules help optimize the communications portion of individual modules. At a later stage, abstract synchronization events are automatically expanded to low-level handshake signals, a step that aims to avoid potential communication mismatches at the signal level. A prototype LISP implementation of the CIPs illustrates the approach on a simple I^2C protocol conversion module.

PARALLEL ALGORITHMS

The second step to effective high-level electronic systems design is translating the high-level description into an efficient implementation, whether it's hardware, software, or both. Problems associated with a single module are generally bounded by today's synthesis tools (for hardware) and compilers (for software). But what if the intended application requires the performance and throughput of parallel computing hardware? Breaking

ENHANCEMENTS ADDED TO PC-BOARD SIGNAL-ANALYSIS AND TIMING TOOLS

With the addition of new algorithms to the XTK design-analysis tool and other enhancements to the Motive timing-analysis tool, Quad Design's pc-board tool suite offers designers expanded capabilities.

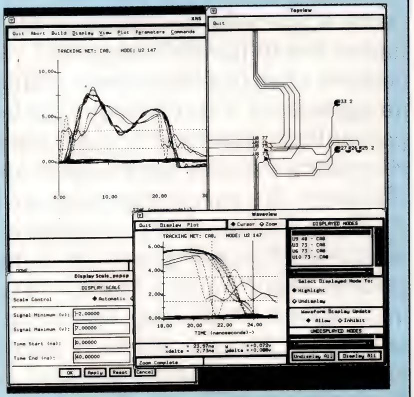
Quad's XTK crosstalk toolkit now includes Monte Carlo analysis, which provides users with a statistical method of predicting worst-case combinations of effects of random parametric variations in semiconductor components. Because Monte Carlo analysis allows exploration of random parameter combinations, it gives higher accuracy than does traditional min-max analysis.

In addition, XTK includes Topview, a layout topology viewer that enables users to graphically view and measure the layout of problem nets independent of the parent pc-board-layout tool. Thanks to this tool independence, users can explore possible layout problems without the expense of pc-board layout-tool licensing.

A multiprocessing capability added to XTK provides a fully automated method of dividing signal-integrity analyses for parallel processing across multiple, networked processors. This reduces processing time and adds the benefit of a single, cohesive report that combines results from all utilized processors.

Various enhancements added to the Motive timing verifier include Global Slack reporting, improved timing-model generation, new I/O-path tracing capabilities, and advanced support for fine-geometry ASICs.

Global Slack is a quantitative measure of how much delay can be added to or subtracted from a net or pin without causing a violation. Motive's comprehensive reporting feature specifies the Global Slack on every datapath device-input pin in the design. With this feature, users can pinpoint the most critical nets and components and thereby bypass the tedious process of reviewing the "n-worst" paths.



Scale Control ◆ Automatic
Signal Minimum (v): -2.00000
Signal Maximum (v): 7.00000
Time Start (ns): 0.00000
Time End (ns): 40.00000

x = 23.97ns y = +0.072v
xdelta = 2.73ns ydelta = +0.000v

The tool's enhanced timing-model generation and I/O tracing is the result of an improved algorithm that provides more visibility to primary input and output calculations. Users are able to tightly monitor and optimize the timing-model generation process, and trace delays forward from primary inputs.

Fine-geometry ASICs now are supported by a distributed RC interconnect delay calculator. When combined with the parametric modeling enhancements made to Motive's ASIC-delay equations, the delay calculator provides a good fit to foundry delay equations.

Ease-of-use features include the ability to interactively scale all delays and constraints. In addition, clock-reference and multicycle-path files support regular expressions and bus notation.

The XTK crosstalk toolkit is available immediately. Pricing begins at $21,000, depending on platform and configuration. Beta shipments of the enhanced Motive tool also are available. Pricing starts at $16,000, depending on the platform.

Quad Design Technology Inc., *1385 Del Norte Rd., Camarillo, CA 93010; (805) 988-8250.* **CIRCLE 604**

■ *Booth 735*

down an application for multiple, parallel resources expands the number of possible solutions.

A paper in Session 30 from the Dept. of Computer Science at the University of Notre Dame, Ind., presents a specialized technique that makes use of parallel computing resources when pipelining loops within an application. This technique can be particularly important in optimizing computing systems for end-user applications like image processing and fluid mechanics. Such compute-intensive applications depend on time-critical sections comprising a loop of instructions. Optimizing the execution rate of the applications requires exploiting parallelism embedded in the repetitive patterns of the loops. The paper, called "Loop Pipelining for Scheduling Multidimensional Systems via Rotation," expands previous work done on one-dimensional (non-parallel) problems to address scheduling multidimensional loops within the resource constraints.

PC-BASED VHDL SIMULATOR UPS SPEED AND SUPPORTS WINDOWS NT

Release 4.2 of Model Technology's V-System/Windows VHDL simulator not only runs much faster than previous versions, but now also supports the NT operating system. V-System includes a VHDL compiler, interactive simulator, and language debugger. It supports the entire IEEE 1076-1993 VHDL standard, and adheres to the 2.2b version of the Vital modeling specification. Vital defines a standard set of semantics to follow when creating VHDL library components.

Speed improvements range from a minimum of 5X on purely structural VHDL designs to as much as 75X on behavioral designs. The average increase is 10X for a typical mixed-level VHDL design. The speed basically results from two enhancements: the full implementation of the company's direct-compile technology, and the conversion of the simulator into a 32-bit application. Direct-compile technology boosts performance by eliminating the CPU overhead required for an interpreted simulator approach.

V-Systems/Windows runs on PCs under Windows 3.1 and Windows NT without modification. It's available now for $2495.

Model Technology Inc., *8905 S.W. Nimbus Ave., Suite 150, Beaverton, OR 97005; (503) 641-1340.* **CIRCLE 605**

■ *Booth 1345*

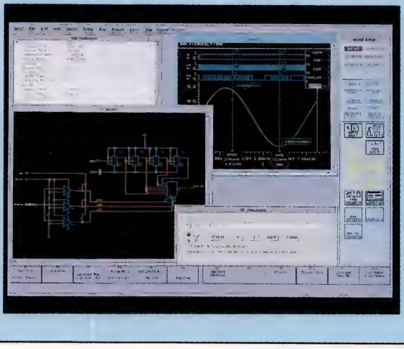
ENHANCEMENTS AID IN MIXED-SIGNAL AND VHDL-BASED SIMULATION

Two announcements from Mentor Graphics improve mixed-signal and VHDL-based simulation, respectively. First, the company is introducing Continuum, an integrated mixed-signal simulation environment based on backplane technology. The second announcement is a set of enhancements to its VHDL simulator.

Continuum meshes analog and digital simulation into one consistent, easy-to-use system. The product provides TTL and CMOS boundary models to support most mixed-signal design technologies. Users also can develop their own custom boundary models for any of their special design needs.

Most mixed-signal products use glued approaches that loosely connect separate analog and digital simulators. However, the Mentor approach brings the two engines together as one simulator with the company's new FlexSim simulation backplane. FlexSim employs the SimView interface to front a variety of simulation algorithms, including VHDL, Verilog, and hardware acceleration. Third-party simulation kernels can be integrated with the FlexSim simulation backplane through Mentor's OpenDoor program.

The SimView interface ties the algorithms together and presents them to users as one tool. And SimView is the same interface used in Mentor's existing digital and analog simulators. As a result, users familiar with either of these products already know how to operate the other.



Other news from Mentor comes in the form of enhancements done to its QuickVHDL simulation family. The VHDL tools have new model support, improved debugging, IEEE 1076-1993 support, and a 30% reduction in cost. In addition, the VHDL software is now integrated with System Architect and Design Architect, the company's system-level design tools.

The Mentor tools run on Unix workstations. Continuum will be available in July. The $65,000 price tag includes analog and digital simulation algorithms, and the CMOS and TTL boundary model library. Pricing for the various QuickVHDL packages range from $14,950 to $45,000. Call for information.

Mentor Graphics Corp., *8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (503) 685-7000.* **CIRCLE 606**

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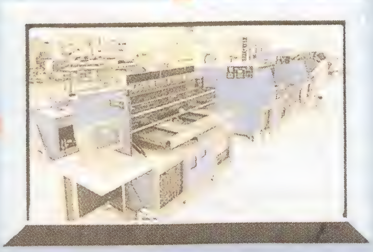

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Beginning with a multidimensional dataflow graph (MDFG), the technique uses a feasible linear schedule to restructure the loop without altering data dependencies. The resulting iterations of the loop make explicit any existing parallelism. Then, with a new technique called multidimensional rotation scheduling, the authors are able to find the optimum retiming for the loop, taking into account the multidimensional resource constraints.

In short, the algorithm finds the best way to schedule operations in a loop across multiple processing resources. How effective is it? The authors applied the method to two examples: a two-dimensional transmission-line problem and an infinite impulse-response (IIR) filter design. With one adder and one multiplier as resources, the multidimensional rotation scheduling reduced seven control steps down to four in the first example. In the second, more complex example, the IIR filter loop was cut from ten steps to eight. In both cases, the authors of the paper demonstrate how the method achieves an

SYNTHESIS TOOL SUITE AND PRINTED-CIRCUIT-BOARD LAYOUT SOFTWARE RUN ON A PC UNDER WINDOWS NT

Three different products make up the VeriBest Synthesis tool suite from Intergraph that runs on Unix workstations as well as PCs under Windows NT. The company also is announcing its VeriBest PCB Designer pc-board layout tool for Windows NT.

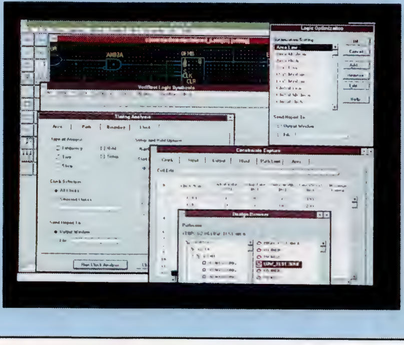
The VeriBest synthesis suite consists of the ArchSyn, MacroSyn, and LogSyn tools that resulted from the combined resources of Intergraph and AT&T Bell Labs. ArchSyn is a behavioral synthesis tool that creates gate-level net lists from hardware-description-language (HDL) modeling. More specifically, it accepts high-level descriptions in VHDL, Verilog, or C, and synthesizes them using such options as resource sharing and allocation. The result is technology-independent net lists that can be used with other VeriBest synthesis tools, or exported to third-party tools.

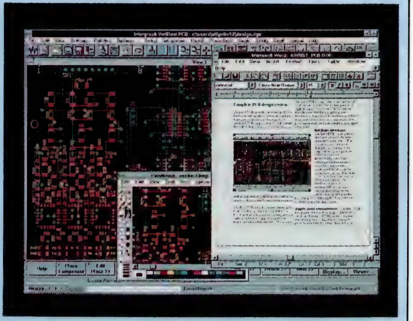
MacroSyn is a template-driven synthesis tool that builds gate-level net lists from both HDL models and user-specified macro parameters. It's targeted at the modular design specification of macros to maximize design reuse. Engineers use a graphical menu to select logic or macro blocks, and specify corresponding I/O parameters and control functions. Using that information, MacroSyn generates schematic symbols, Verilog or VHDL simulation models, and gate-level net lists.

The macro blocks include commonly-used functions like adders, counters, comparators, and multiplexers. MacroSyn also can synthesize finite state machines from state tables and state languages, and can create random logic from truth tables and equations. When defining these blocks, users specify parameters such as width, and select-clocking, control, and implementation options.

LogSyn provides optimization and analysis for circuit refinement *(see the photo, bottom)*. It employs target-library information and user constraints to refine a circuit for area and performance requirements. A hierarchy manager lets users mark by instance or by type to control the action of the optimization engines. In addition, a net-list partitioner can split a large, complex design into small, manageable blocks.

VeriBest PCB Designer is a layout tool used for the design, analysis, and manufacture of high-density, mixed-technology boards *(see the photo, top)*. The software supports low- to high-density through-hole technology, as well as high-density, surface-mounted designs with either single- or double-sided component mounting.





Engineers can perform interactive, auto-interactive, and batch routing. Product features include shape-based routing, dynamic push-and-shove routines, automatic test-point generation, and user-configurable report generation. With a flexible and open database, users can generate outputs to drive any software or machinery.

The VeriBest PCB Designer software is integrated with Intergraph's Electronics Desktop Manager (EDM) environment. EDM lets users perform operations by using drag-and-drop techniques. In addition, it provides integration across data and applications, and easy access to all network peripherals and processes. EDM also provides an integrated graphical work-flow-generation and editing tool called Design Methodology Manager (DMM).

Contact Intergraph for pricing and additional information.

Intergraph Corp., Huntsville, AL 35894-0001; (205) 730-8577. **CIRCLE 607**
■ *Booth 1401*

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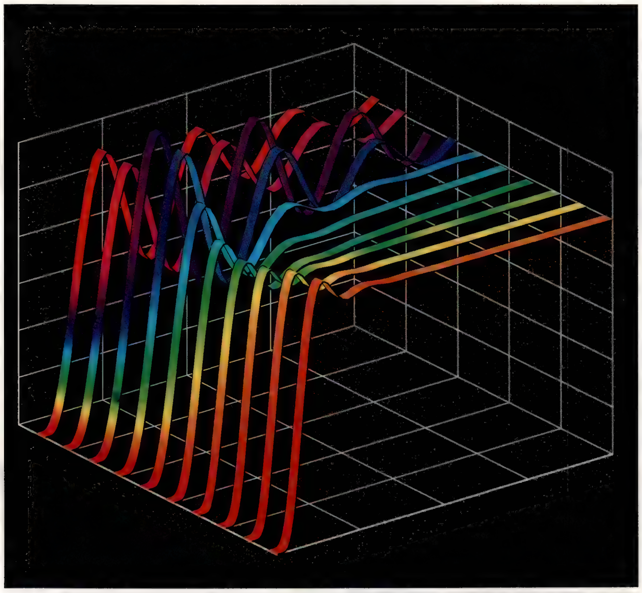

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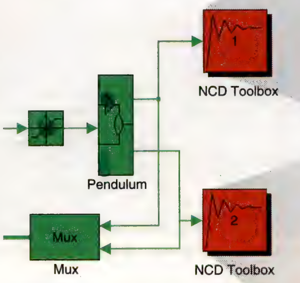

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Using your mouse, you simply point-and-click to place constraint bars on a time response plot to shape your system's output. Then press the "start" button to automatically tune your controller and satisfy the performance objectives — rather than guessing values for a weighting matrix. What once took hours or even days now takes just a few moments.

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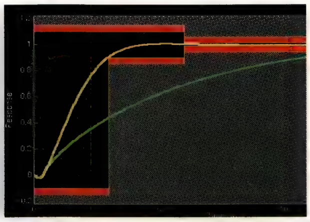

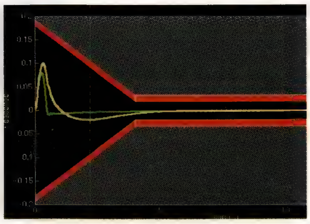

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Total # of Gates	330	2,000	660	2,000	4,000	6,000	10,000	14,000	18,000	22,000	32,00
# Usable Gates	270	1,800	600	1,800	3,600	5,400	9,000	12,600	16,200	19,200	28,80
Commonly Used Packages	16SOIC	20SOIC	44PLCC	68PLCC	84PLCC	100PQFP	128PQFP	144PQFP	160PQFP	160PQFP	208PQ
	14SOIC	16SOIC	28PLCC	44PLCC	68PLCC	84PLCC	100PQFP	100PQFP	144PQFP	144PQFP	160PQ
		14SOIC	20SOIC	28PLCC	44PLCC	68PLCC	84PLCC	84PLCC	100PQFP	100PQFP	144PQ
			16SOIC	20SOIC	28PLCC	44PLCC	68PLCC	68PLCC	84PLCC	84PLCC	100PQ
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optimal result.

Engineers can find more papers relating to the development of hardware components in DAC's many synthesis sessions. For example, software modules are discussed in "Software and Instruction Set Synthesis" in Session 2. In fact, the whole issue of synthesis from high-level descriptions may be the most discussed topic at the show. For the high-level perspective, the panel in Session 13, called "ESDA and Design Abstraction: How High is Up?," will have ESDA system developers discuss the successful use of focused, domain-specific ESDA tools, and the trade-offs between domain-specific and general-purpose ESDA.

SYNTHESIS CHANGES

Synthesis topics have remained at the core of DAC for years because it's been the technology base behind the higher levels of design abstraction. DAC sessions and papers have consistently revealed the forefront of synthesis for the industry. In 1994, engineers will see how synthesis has expanded across the range of design problems—both in terms of raw power and in terms of addressing the needs of specific design methods and implementation technologies.

While early synthesis tools conquered the limited solution space of combinatorial circuits, the industry continually struggles to develop efficient algorithms for sequential circuits (referred to as finite state machines). The problem is simple: the number of potential states in a finite state machine (FSM) grow exponentially with the number of registers. Explicit methods to find a minimized implementation of an FSM grind to a halt from trying to keep track of the state-transition graph.

Recent research has shown how synthesis programs can bypass the transition graph and, instead, compute a class of equivalent states implicitly. In fact, equivalence classes are all that's needed to minimize a completely specific state machine. In the paper "A Fully Implicit Algorithm for Exact State Minimization," in Session 42, researchers at the University of California at Berkeley show how to extend the implicit tech-

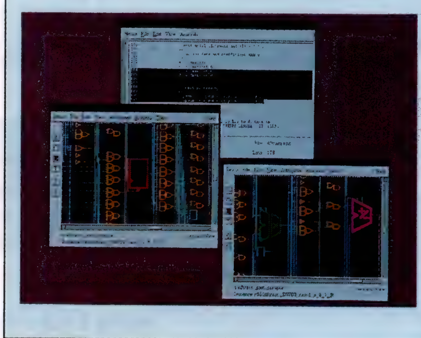
BEHAVIORAL SYNTHESIS CREATES ICS FROM ALGORITHMIC DESCRIPTIONS

Behavioral Compiler from Synopsys is a high-level synthesis tool for IC design. The company took a new approach to behavioral synthesis, making the tool valuable for virtually any design that's best described by an algorithm. These types of applications are found most often in telecommunications, high-end graphics, and multimedia.

With behavioral synthesis, engineers specify a circuit's behavior at a high level of abstraction in Verilog or VHDL, without detailing the exact architecture. The synthesis software then optimizes the design to meet performance goals while minimizing chip area.

Until now, most behavioral synthesis research has focused on datapath design and scheduling. But Synopsys' software goes beyond scheduling, incorporating capabilities like controller inferencing, memory inferencing, and integration with architectural and logic synthesis.

Behavioral Compiler synthesizes descriptions whose cycle-level activity hasn't been completely defined, or that might be changed to meet optimization goals. It schedules operations, such as additions, multiplications, memory reads, and memory writes, into a set of control steps (cycles). The compiler also performs multicycle hardware allocation for operators, registers, and multiplexers. Using this schedule and hardware-allocation information, Behavioral Compiler automatically synthesizes a controller for the entire design.



Many ASIC design teams start with an algorithmic specification in C or C++ combined with target performance levels. From there, engineers manually schedule the design and hardcode a lengthy register-transfer-level (RTL) specification. With Behavioral Compiler, engineers can write a behavioral specification that's similar to the original algorithm. Moreover, the behavioral description can be up to 10 times shorter than an RTL specification for the same application.

Behavioral Compiler then automatically infers the design's controller from the specification. This means that users don't have to specify the controller and integrate it with the datapath by hand. The result is a much shorter specification.

The behavioral synthesis tool also automatically infers memory reads and writes from HDL array accesses, which means that it can automatically schedule memory access. Consequently, users no longer have to spend lots of time working on tedious memory timing and scheduling issues. In fact, Behavioral Compiler has three scheduling modes, affording users as much or as little control over the design timing as they desire.

Users can enter both Verilog and VHDL descriptions. Behavioral Compiler makes use of both the company's architectural-synthesis and logic-synthesis tools. Engineers can also use the DesignWare libraries of synthesizable pre-defined funtions.

Behavioral Compiler runs on Unix workstations. Pricing is set at $69,500. Production shipments are scheduled for the fourth quarter.

***Synopsys Inc.,** 700 E. Middlefield Rd., Mountain View, CA 94043-4033; (415) 962-5000.* **CIRCLE 608**

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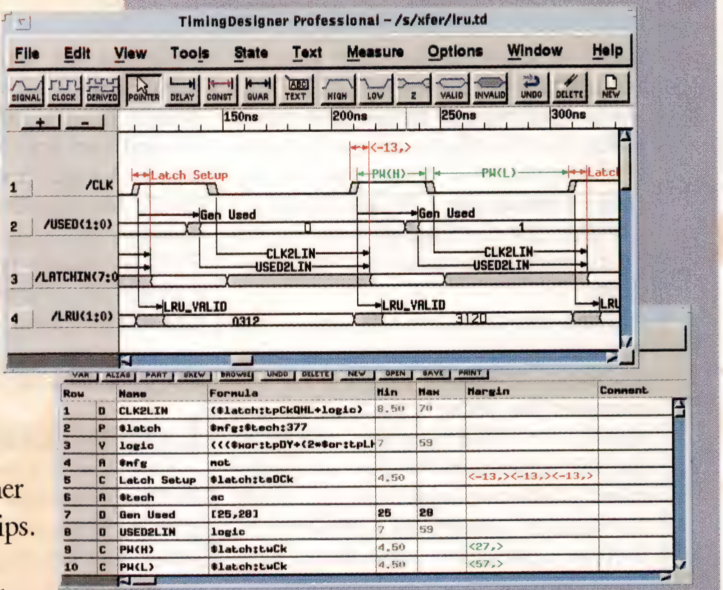

Row		Name	Formula	Min	Max	Margin	Comment
1	D	CLK2LIN	($latch:tpCkQHL+logic)	8.50	70		
2	P	$latch	$mfg:$tech:377				
3	V	logic	((($xor:tpDY+(2*$or:tpLH	7	59		
4	A	$mfg	not				
5	C	Latch Setup	$latch:tsDCk	4.50		<-13,><-13,><-13,>	
6	A	$tech	ac				
7	D	Gen Used	[25,28]	25	28		
8	D	USED2LIN	logic	7	59		
9	C	PW(H)	$latch:twCk	4.50		<27,>	
10	C	PW(L)	$latch:twCk	4.50		<57,>	

ke Corporation

designs consist primarily of micros, RAM, DRAM, and plex peripheral chips on PCBs. I have found TimingDesigner nearly perfect for analyzing the interfaces among these chips. only other choice I have is: paper, pencil, calculator, and to all over from the top every time I make a change. I was able to tarted with my work as soon as I got the software. I didn't have to open the manual."

n Witters, Staff Engineer

Network Peripherals

"I'm a big user of Xilinx FPGAs. I use TimingDesigner, heavily, at two steps in my design process. At the start I use it to investigate design alternatives. This gives me an idea of my timing budget—and that drives many of my design decisions. Later on, when I have a completed Xilinx design with actual routed chip delays, I use TimingDesigner to make certain the chips will work with the surrounding merchant chips. It really helps me find solutions to knotty timing problems."

- Sandy Helton, Design Engineer

n Microsystems

use Motive, Synopsys, TimingDesigner, and Verilog to design 1-performance graphic accelerator chips. When we begin the gns, we use TimingDesigner to check vendor VRAM timing lels against the chip design constraints. When we make nges, the first thing we do is look for any "red" in the diagrams. ingDesigner provides the waveforms for a fast and easy visual ysis of the interface between our chips and the surrounding chant parts."

eve Chiou, Hardware Engineer

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nique to cover an FSM with an enormous number of compatibles, which are sets of related states. The paper claims the technique can handle up to 2^{1200} compatibles. Moreover, the authors present the first published algorithm for the final step in the implicit exact-state minimization procedure.

Their reported results prove the capabilities of this approach to solve synthesis problems that are far too complex for today's state-of-the-art minimizers. This paper sets the foundation for others trying to implement state minimization and other variants of sequential synthesis, as well as approaches associated with logic synthesis and combinatorial optimization.

After logic synthesis, most design-automation environments perform optimization on a design to take advantage of technology-specific structures in the target ASIC's library. By adding field-programmable gate arrays (FPGAs) to the synthesis design flow, similar optimization is beginning to appear for these devices. However, the problem with FPGAs usually isn't with logic utilization, but rather with wiring utilization. FPGA designs often run out of interconnect resources before they use up all available logic.

LAYOUT-DRIVEN SYNTHESIS

That's why researchers at AT&T Bell Laboratories, Murray Hill, N.J., and the Dept. of Electrical and Computer Engineering at the University of California at Santa Barbara developed a layout-driven synthesis approach for FPGAs. This approach, presented in Session 20, attempts to identify in the logic layer alternative wires and functions for existing wires in the design. That way, when an existing wire can't be completed due to limited FPGA routing resources, it's replaced with an alternative wire or function. Alternative wires can be routed through less-congested areas to replace unroutable wires without changing the circuit's functionality. On the other hand, alternative functions simply change the wiring requirements altogether.

The paper presents redundancy addition and removal techniques used to identify the alternative wires. The authors found that 30 to 50% of wires have alternates, a result which suggests that routing flexibility can increase substantially when considering the alternates. In fact, a prototype system embodying this technique completed the routing

SIGNAL-PROCESSING ENVIRONMENT ADDS FEATURES FOR WIRELESS DESIGN

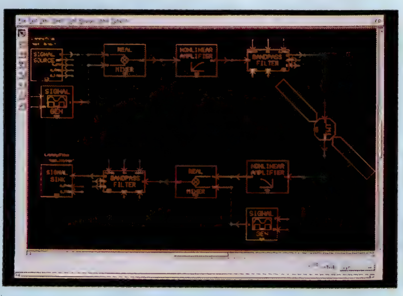
The Signal Processing WorkSystem (SPW) tools developed by the Alta Group of Cadence Design Systems include three new features aimed at simplifying wireless-communications design. First, the Fixed Point Optimizer automatically determines the optimum fixed-point attributes of a behavioral algorithm and/or architectural design. Next, a multirate feature speeds up high-level system simulations. Lastly, an RF block library broadens the environment for wireless communications design. All of the tools run on Unix workstations.

Fixed Point Optimizer works with the company's Hardware Design System, which is an SPW option for accelerating DSP hardware design. It will optimize fixed-point attributes for any kind of system, including the time-varying, multirate, and nonlinear systems that are common in wireless communications and multimedia products.

Using the tool, engineers can optionally start with a floating-point system, and then automatically replace floating-point blocks with their fixed-point equivalents. Based on the user's optimization goals and input signals, the Fixed Point Optimizer will minimize the number of integer bits in a word so that dynamic range is maximized without arithmetic overflow. The Fixed Point Optimizer will ship in the third quarter for $20,000.

A multirate simulation feature added to SPW simplifies design capture for wireless and multimedia applications. In addition, multirate simulations run faster than event-driven or dynamic-dataflow simulations because there's no run-time-scheduling overhead.

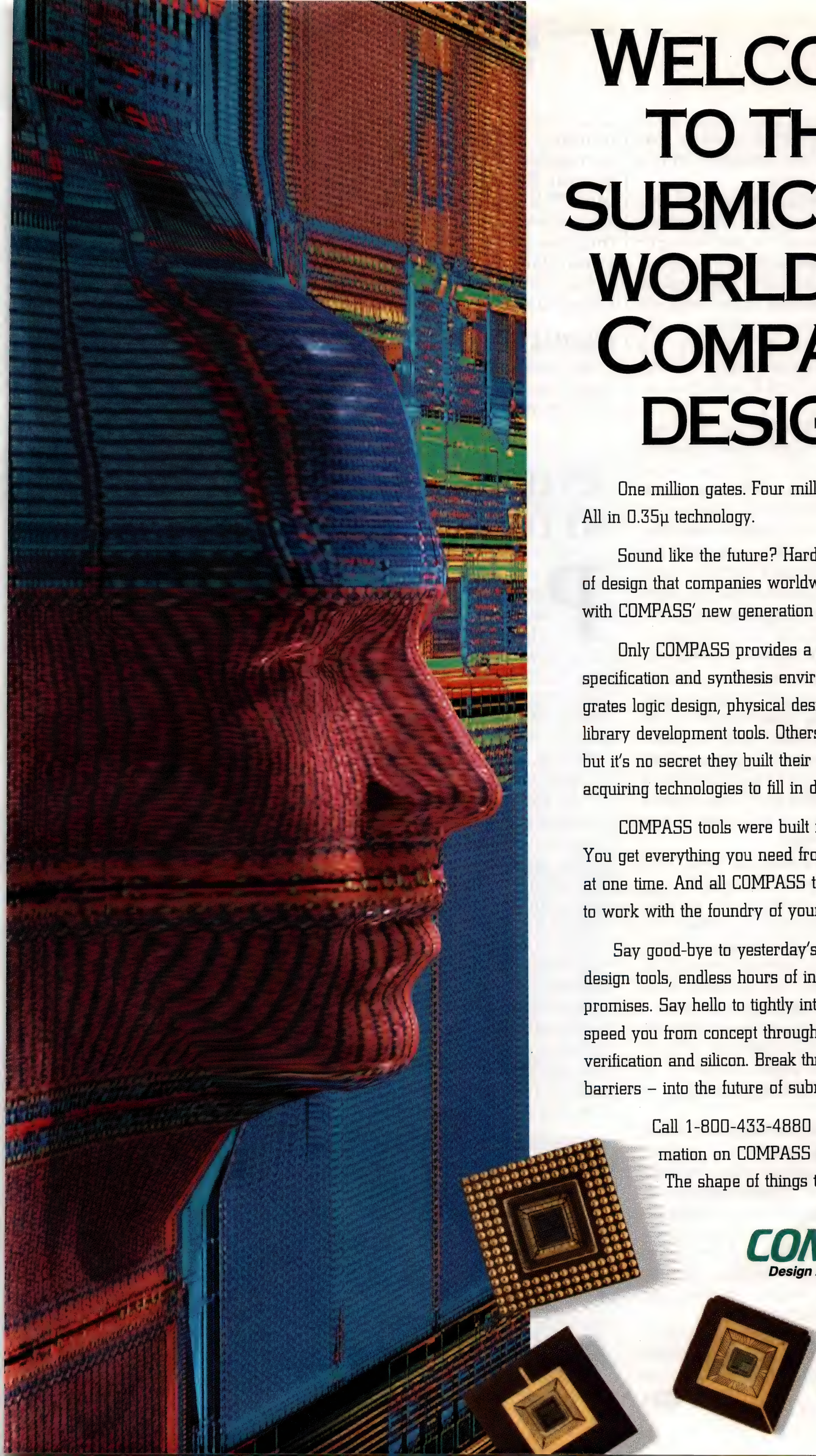
Within a system model, users designate one point as having a specified reference sampling rate. The simulator and code generator then use this reference to automatically calculate and maintain all other sampling rates within the system model. The multirate feature is included in SPW 3.1, which is available now. Pricing for the SPW system starts at $25,000.



The RF library expands the capabilities of the SPW design environment. Until now, DSP simulation hasn't been available for RF amplifiers, mixers, and other non-ideal components found in radar and wireless communications. The RF library is a collection of blocks for modeling the radio-frequency portion of a signal-processing system. It reveals the impact that nonlinearities and interference introduced by real-world components have on system performance. Included in the library are: nonlinear amplifiers, switches, couplers, analog-to-digital converters, and mixers. The RF library will be available in the third quarter for $5000.

Alta Group of Cadence Design Systems Inc.*, 919 E. Hillsdale Blvd., Foster City, CA 94404; (415) 574-5800.* **CIRCLE 609**

■ *Booth 701*



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of two AT&T FPGA designs that failed in previous attempts with a normal FPGA router.

The greater significance of this technique is that the alternatives also can be considered for timing or density parameters, as well as interconnectivity. All such applications explore alternatives in the logic domain that improve results in the physical domain. In addition, the technique can be adapted to the design of standard-cell ICs and gate arrays.

DAC also is showcasing how synthesis is being augmented to support particular design techniques, such as scan testing. But FPGA technology and scan testing are just two areas in which synthesis is specializing. Session 2, for instance, discusses software and instruction-set synthesis. Engineers also can learn about the latest in synthesis of asynchronous circuits in Session 6, memory structures in Session 10, and datapaths in Session 14. In fact, DAC attendees can see new ideas in many arenas, ranging from high-level synthesis (Session 34) to layout and technology-independent synthesis (Session 22). At almost every turn, engineers are finding synthesis expanding its role to further streamline their design cycles.

ESDA and synthesis aren't the only areas affected by today's large designs. For example, as product complexity skyrockets, it drags the problem of testability along with it. How does a company ensure comprehensive testing for products with millions of transistors and restricted access? To make matters worse, engineering teams are looking for testing with even higher coverage to meet heightened expectations of quality.

The increasing activity concerning testability and test-vector generation is spread across many sessions at the 1994 DAC. These sessions reveal the ongoing work in making design-for-test techniques more accessible, more effective, and less obtrusive. New algorithms automatically generate test vectors quicker and with higher coverage.

Scan testing is a popular technique for increasing test access within dense IC and ASIC designs. The scan technique involves replacing internal registers with modified versions that can link together via a serial path. This serial path—called the scan path—becomes a means for setting the internal registers to a known state, and for reading an existing state out of a device, all through a handful of pins.

PARTIAL SCAN

The trade-off in scan design is the larger size and the slower operation of the modified registers. For some time- or area-constrained circuits, engineers can't afford the luxury of replacing all registers with scan versions. In these cases, they want to insert only enough scan registers to ensure target coverage levels. Determining this optimum number of scan registers in a large circuit is difficult, if not impossible, even with the help of design automation.

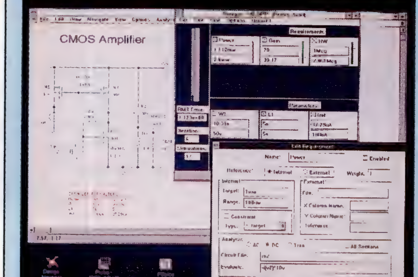
In response, researchers at the Computers and Communications Research Laboratories of NEC USA Inc., Princeton, N.J., are presenting

ANALOG CIRCUIT OPTIMIZER WORKS AT THE SYSTEM AND COMPONENT LEVEL

Performance of analog circuits at both the system (behavioral) and component levels can be improved with the Paragon optimizer created by MicroSim. Paragon is offered as an option to the company's Design Center mixed-signal design environment, which includes schematic capture, simulation, and analysis.

The Paragon software performs iterative simulations, adjusting parameter values until performance goals and user-specified constraints are met. For example, Paragon can compute the parameter values for an active filter design that will meet the designer's center-frequency, bandwidth, and gain requirements.

Automatic performance optimization adjusts all design parameters for each successive simulation, eliminating the painful process of manually tweaking parameters one at a time. It also reduces the total number of possibilities to be investigated.



Interactive circuit exploration with graphical feedback lets users examine performance trade-offs when manually changing one or more design parameters in a working circuit. It also can be used when exploring how the changing performance requirements will affect design parameters. A model-parameter fitter adjusts model parameters to measured data.

Tight integration with the Design Center makes using Paragon easy. After design entry and simulation, design parameters, performance requirements, and optimization constraints (including nonlinear constraints) are defined with dialogue boxes. Once Paragon satisfies all of the requirements, component values are rounded to manufacturers' standard values. Finally, the schematic is back-annotated with the optimized parameter values.

Paragon will be available by the end of July. It's offered as an option to the Design Center on both PCs and Sun workstations. Pricing is set at $1900 and $3900, respectively. A 25% introductory discount is in effect through September.

MicroSim Corp., 20 Fairbanks, Irvine, CA 92718; (800) 245-3022 or (714) 770-3022. **CIRCLE 610**

■ *Booth 313*

a paper in Session 7 titled "Resynthesis and Retiming for Optimum Partial Scan." The authors' approach starts with a graph of the signal dependencies among the flip-flops called a FF dependency graph. To find an optimum partial scan implementation, the technique finds the minimum set of those flip-flops (called the minimum feedback vertex set, or MFVS) that contains no signal loops, except for self loops. To reduce the size of the MFVS, which would minimize the number of required scan registers, the technique uses resynthesis to break all loops in the FF dependency graph. It then employs retiming to minimize the combinatorial and sequential logic overhead required for the new circuit structure.

To prove the approach, the authors implemented the algorithm in a program called RROPS (retiming and resynthesis for optimal partial scan). In numerous benchmark circuits, RROPS significantly reduced the MFVS with only marginal increases in overall circuit size. In addition, the authors compared RROPS results with those of four other methods for selecting scan flip-flops. The experimental results clearly showed a significant reduction in the number of required scan registers using RROPS.

Once a circuit has all testability structures built in, engineers must turn to the task of test-vector generation. Automatic test-pattern-generation (ATPG) programs exist in the commercial marketplace, each of which can help engineers augment functional vectors, with vectors aimed at specific locations and fault types. Existing solutions, however, often are based on assumptions and techniques arising from previous generations of designs. Today's circuits already contain densities and complexities that can drive up these solutions' execution times and lower their fault coverage. Several papers at DAC demonstrate the continuing effort to improve the efficiency and effectiveness of automatic-test-pattern-generation programs.

SIMULATION TOOL DETECTS EMC PROBLEMS IN HIGH-SPEED SYSTEMS

The problems associated with electromagnetic compatibility (EMC) and designing to reduce EMI are complex. They're important, however, because the FCC and European community are proposing new regulations that will make EMC a primary consideration in system design.

To that end, the Compliance EMC-simulator design tool helps engineers actively solve EMC problems during the design process. The tool intends to eliminate system redesigns that are brought on by prototypes that fail EMC testing. Both FCC and CISPR 22 standards are supported.

A complete analysis of a system's EMC status should accommodate common-mode currents as well balanced-current radiation. Not only does the Compliance tool take common-mode currents into account, but it also calculates radiated fields from systems of printed-circuit boards and from common-mode currents on all cables and enclosures.

The simulator uses time-domain current waveforms on transmission lines for nonlinear devices, and frequency-domain analysis for assessment of electromagnetic radiation. Because the source of radiation often is at the board level, signal ringing resulting from mismatches and long signal paths must be addressed. To achieve that goal, the Compliance tool is integrated into the company's Signal Integrity tool set, which includes the BoardScan and Greenfield tools for convenient exchange of data. Call the company for pricing and delivery information.

***Quantic Laboratories Inc.**, 191 Lombard Ave., 12th floor, Winnipeg, Canada, R3B 0X1; (800) 665-0235.*

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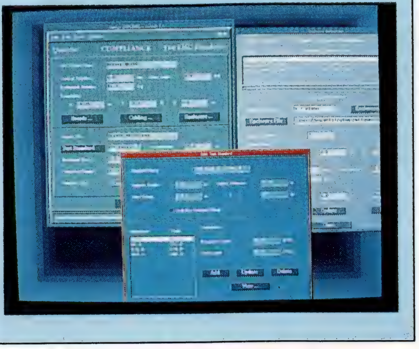
■ *Booth 243*



For instance, consider a best-paper candidate from researchers at Sunrise Test Systems Inc., Santa Clara, Calif., and the Coordinated Science Laboratory at the University of Illinois at Urbana-Champaign. The paper shows how they applied Genetic Algorithms (GAs) to test-pattern generation in sequential circuits. Effective in many categories of search and optimization problems, Genetic Algorithms can evolve (modify) candidate test vectors using a fault simulator to compute the fitness (ability to detect faults) of each candidate test.

In this paper, the authors extended the GA approach to evaluate test sequences as well as individual vectors. Their GA evolution is modeled after biological precedents. Populations of chromosomes that represent the test vectors are modified by evolutionary operators. Typically, the initial population is randomly generated. It's then evolved by selecting two individuals, crossing them, and mutating the results according to mutation probability. A sequential fault simulator then judges the effectiveness of the new population.

Results of this approach are promising. In most of the paper's example cases, the test-generation time for a GA-based generator was just a small fraction of the time needed by a more traditional sequential-circuit test generator. The authors conclude that the present incarnation of this approach is appropriate for a first-pass test generator to screen out many faults before applying a deterministic test generator.

Concerning deterministic test generators, another paper, "Dynamic Search-Space Pruning Techniques in

DFM CONFERENCING SOFTWARE SUPPORTS REAL-TIME INTERACTION BETWEEN MANY DIFFERENT SITES

Engineers at multiple sites can perform design-for-manufacturability (DFM) analysis on the same board with conferencing software from AT&T Design Automation. The Electronic DFM (EDFM) Conferencing product allows for real-time electronic sharing of AT&T's workstation-based DFM applications over existing TCP/IP networks using low bandwidth lines.

With EDFM Conferencing, design and manufacturing engineers at geographically dispersed locations can simultaneously view and edit information on their screens. The software generates a textual output that can be used as review documentation.

The host location requires an AT&T DFM product license and a host conferencing port, while remote locations need only the remote conferencing station software. Up to ten remote and one host location can be supported in one conference.

Setting up the EDFM conference is not difficult. The design-data file, which is an ASCII file with both text and graphics, is sent over the network from the host to other locations. This is typically done before the conference. During the actual review, the DFM Conferencing software is sending actual application data so that the remote locations can see changes instantly. This is in contrast to other workstation-based conferencing products that just swap single screen images back and forth.

The AT&T EDFM Conferencing software will ship in the third quarter for HP and Sun workstations. The host port costs $3500, and each remote station goes for $4500. Volume discounts apply. Training and support is available from the company.

***AT&T Design Automation**, 101 Crawfords Corner Rd., Holmdel, NJ 07733; (800) 336-5256.* **CIRCLE 612**

■ *Booth 1235*

ASIC TEST TOOL AUTOMATES BIST STRUCTURE CREATION

A complete solution for front-end generation of synthesizable BIST/1149.1 structures and back-end test synthesis and test-pattern generation is provided by the ASICTEST family of test-automation tools. The family helps users incorporate design-for-testability (DFT) and built-in self-test (BIST) in their ASICs.

With built-in self-test, IEEE 1149.1 test access port and boundary scan, internal scan, and other test concepts, the ASICTEST family lets engineers selectively apply testing techniques in a unified manner to generate efficient and effective test methodologies.

At the tools' heart lies the concept that engineers should have complete control over the testability aspect of ASICs at an early point in the design flow. Such control would make it easy to optimally mix different DFT methodologies. The program achieves this through such features as generation of BIST modules for embedded RAM, complete generation of an IEEE 1149.1-compliant top-level module, and flexible scan-chain insertion. It also provides fast combinational test-pattern generation and integration of test data and test objects across all products.

Products in the ASICTEST family include ICRAMBIST for built-in self-test of embedded RAMs in ASICs; JTAGSYN for IEEE 114.1 test access port and boundary scan; and ICSCANTEST for scan-chain insertion, combinational ATPG, and fault simulation. Call the company for pricing and additional product information.

***LogicVision Software Inc.**, 1590 Oakland Rd., Suite B-205, San Jose, CA 95131; (408) 453-0146.* **CIRCLE 613**

■ *Booth 137*

Path Sensitization," discusses a new method for finding a set of values that locate faults on a specific path. One exciting prospect of this approach is that it has a linear time complexity, as opposed to well-known alternatives that exhibit worst-case quadratic time complexity. In other words, as design complexity grows, computational requirements for this approach increase at a much slower rate than those of other approaches. Moreover, path sensitization has application in delay-fault testing and timing analysis, as well as test-pattern generation.

The existence of Design Automation Conference Session 43, devoted solely to test generation, underscores the ongoing integration of design and test disciplines. What's more, other sessions and papers on design-for-test, fault simulation, and diagnosis will give as much pertinent information to test engineers as they will to design engineers. ☐

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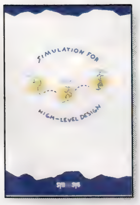

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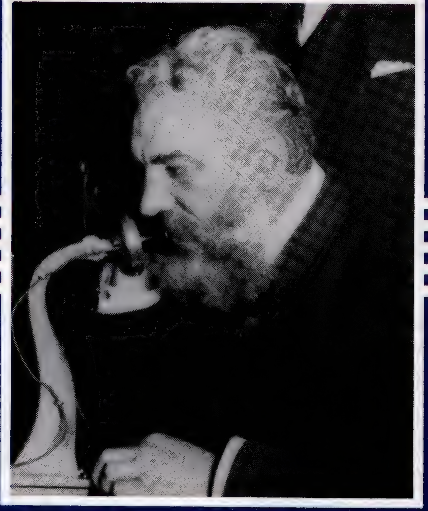

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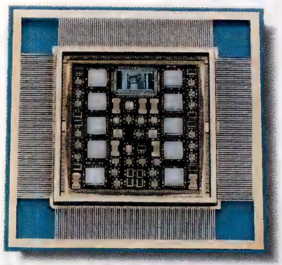

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NIX PHYSICAL DESIGN FLAWS BEFORE LAYOUT

LISA MALINIAK

There's both good news and bad news for engineers designing boards around ultra-fast chips like the Intel Pentium, DEC Alpha, and PowerPC processors. The good news is that they can theoretically run their systems at lightning speeds. The bad news is that building a board which can function properly at such high clock speeds becomes a herculean task.

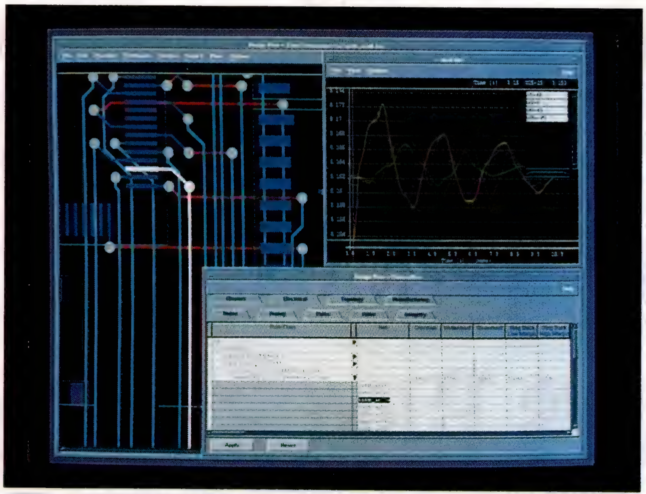
Consider, for example, the hurdles associated with a Pentium-based board. The main design problem is creating a reliable motherboard (memory, video, system bus) that can keep up with the speed of the Pentium processor. Tolerances may also be a problem—with higher speeds, the error margin diminishes dramatically and impacts yield.

Engineers with little or no experience in building high-speed systems might not be able to master the learning curve. Even those that do know how will generate too many design iterations. Finally, the Pentium dissipates lots of power, thus it runs hot. Intel is providing system vendors with thermal models, but engineers will have to pay close attention to fan and component location, because their placement affects timing.

A new company, Interconnectix, aims to help engineering teams go head-on with high-speed pc-board and multi-chip module (MCM) design issues. Its first product, IS, is an interconnect-synthesis environment that attacks signal-integrity and timing problems caused by physical-implementation details. Interconnect synthesis takes a high-level electrical abstraction of interconnects that's defined in terms of timing and signal-purity specifications, and generates a detailed and implementable physical representation that matches the electrical description.

Most of the high-speed-design headaches result from the inability to maintain interconnect-signal integrity. In the past, the limiting factor for system performance was the time it took signals to propagate through devices. But with very-high-speed systems, the primary barrier to system speed and signal integrity is in the interconnect between devices.

Speed problems are exacerbated by the



1. ENGINEERS ENTER signal-purity requirements, such as crosstalk, overshoot, undershoot, and ringing, in electrical terms through the IS spreadsheet-based rules editor. The synthesizer then generates a detailed interconnect representation that matches the signal-purity specifications. In this screenshot, the waveform in the upper-right corner indicates that crosstalk was kept below the 200-mV limit specified in the spreadsheet.

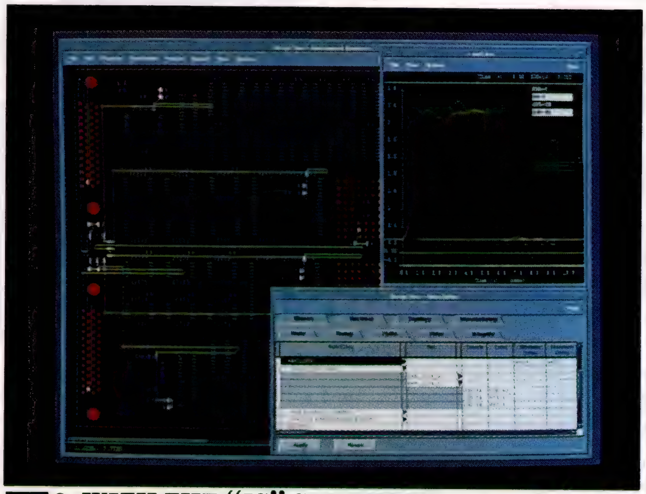
growing complexity of designs and the number of timing-critical interconnects. Instead of a handful of critical pins, engineers now are confronted with thousands of high-speed signal pins in one design. As a result, the effects of impedance mismatches—noise, ringing, overshoot, undershoot, and crosstalk—are the invisible monsters that destroy high-speed designs.

Using the current design methodology and tools, timing and signal-purity issues don't manifest themselves until the design is in the physical-implementation stage, when it's costly and time-consuming to make corrections. To complicate matters, physical implementation is done within a CAD environment that deals with geometry-based constraints. These are foreign to most engineers who think of circuits in electrical terms.

Faced with time-to-market pressures, engineering teams can't wait until the end of the traditional layout stage before identifying interconnect problems that will cripple a design. To remain successful, engineering management must expand its design methodology to confront the problems of high-speed digital design long before it reaches the CAD department. But the increased circuit speed and complexity are breaking the backs of the traditional EDA tools. Existing tools just aren't scalable to today's problems.

Today's engineers basically take two approaches to these problems. Some use post-layout analysis, which requires many time-consuming iterations between the design's logical and physical representations. Others use geometry-based design rules (for example, physical design rules such as length constraints). The latter solution is conservative and expensive, because rigid rules constrain space and performance. Also, designers tend to violate these rules and resort to an auditing process based on post-layout analysis.

Using IS, engineers can assess the timing, electrical, and physical domains before committing the design to CAD. Raising the level of abstraction of the design constraints lets them anticipate and correct problems without costly redesign due to timing and signal-integrity flaws that remained dormant until physical implementation began.



2. WITH THE "IS" SOFTWARE, engineers can manage skew between multiple clocks held within sub-nanosecond requirements. Users interact with the tool using a spreadsheet that's linked to the graphical application with a bidirectional, cross-selection mechanism.

IS is aimed at electrical engineers designing digital pc boards and MCMs. Consequently, a spreadsheet-based input system tightly integrated with graphics-intensive applications specifically addresses the casual usage model. This paradigm requires little or no typing when manipulating design objects or rules.

IS is an X-Window, Unix-based software system that consists of four modules: a hierarchical timing- and thermal-driven floorplanner, a physical-analysis engine, a spreadsheet-based rules engine, and a synthesizer/intelligent router. At its core lies a technology that combines the analysis, rules, and layout-synthesis engines for interconnect synthesis. Internal data models consist of geometrical and analytical data that accurately represents objects for interconnect routing and allows quick access to geometry data for real-time analysis.

Users are offered front- and back-end integration with leading design creation and host CAD/CAM systems. The design is captured in schematic or hardware-description-language (HDL) form, and compiled into a net list of the actual devices to be used in the physical design. IS supports a number of standards for data exchange, including ASCII neutral files for front- and back-end integration, and Standard Delay Format (SDF) files for passing timing constraints. Netlist interfaces are available for Mentor Graphics' Design Architect, Cadence's Concept, and Viewlogic's ViewDraw design-entry systems. Host CAD interfaces include Mentor Graphics' Board Station and MCM Station, Cadence's Allegro, and Racal-Redac's Visula.

Other relevant properties that will affect the synthesis process, such as electrical and thermal models and physical geometries, may

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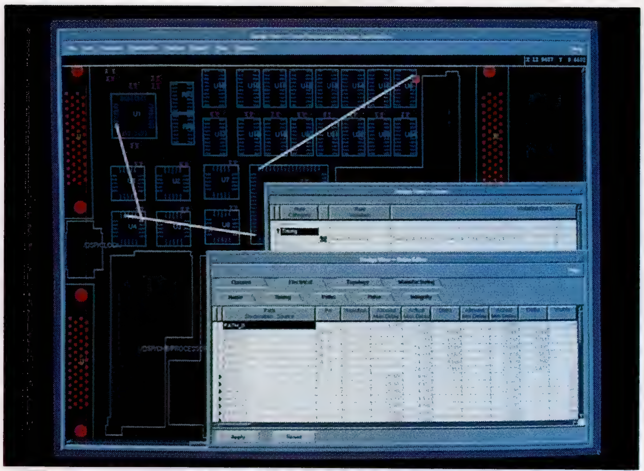
come from technology libraries associated with components used in the design. The Input-output Buffer Interface Specification (IBIS) standard, which is fully supported in its native format, is used to obtain electrical device models.

The IS user-interaction paradigm is based on spreadsheet technology tightly integrated with a graphics-intensive physical-layout module. Engineers use the spreadsheet-based rules editor to specify a set of rules for specific elements or groups of elements (classes) within the design *(Fig. 1)*. These rules can augment constraints brought forward in the form of net-list properties and critical-path data. Timing and signal-purity rules can include setup-and-hold time specifications; path- or net-based time delay; skew management; maximum allowable crosstalk; overshoot and undershoot; and ringback constraints *(Fig. 2)*.



3. THE TIMING-DRIVEN FLOORPLANNER

computes slack allocation in real time for all critical timing paths. With every movement of a floorplan block or component within a block, path timing budgets are redistributed in real time using delay estimates based on detailed device, substrate, and interconnect material models. Violation of setup-and-hold-time specifications are displayed both graphically and in tabular form on the error-report sheet.

The synthesis engine is actually an intelligent router that makes strategic and tactical routing decisions based on user-specified manufacturing design rules and electrical constraints. This process continues until an implementable physical representation that matches the electrical description is found. Real-time transmission-line and crosstalk analysis is possible during the synthesis process because of a single data structure specifically developed to accommodate concurrent analysis and interconnect routing.

For example, the synthesizer adheres to the crosstalk rules specified for a given net by performing crosstalk analysis on that net and its surrounding neighbors. This guarantees that the crosstalk threshold wasn't exceeded while the net was routed. Once completed, a functionally placed-and-routed representation is generated for the manufacturing phase.

The IS analysis engine is made up of parameter-extraction and circuit-simulation modules. The engine operates in two distinct modes: a synthesis mode and an analysis mode. Parameter extraction is based on an implementation of the moments-and-integral equation that the company says is unique. Interconnect simulation is based on time-domain analysis of transmission-line equations, with general nonlinear termination represented by I-V curves.

In the synthesis mode, real-time analysis prioritizes and determines where it's best to lay down interconnects, which are subject to time delay, reflection, overshoot, undershoot, and maximum-crosstalk constraints. The IS analysis engine provides accurate and fast electrical analysis, making it possible for users to detect signal-integrity violations, display waveforms, and perform what-if analysis on design alternatives. The physical-analysis engine and the rules engine work in unison to create real-time synthesis rules.

The IS synthesizer is complemented by a timing-driven hierarchical floorplanner. The two work together to ensure that setup-and-hold time requirements and signal-purity thresholds won't be violated. Violations arise from additional delay introduced by interconnects in the physical realization of the design.

Large numbers of speed-critical nets within complex pc-board and MCM designs require timing-driven, hierarchical floorplanning. This allows design decisions and changes to be made at an architectural level, rather than dealing with hundreds of components and thousands of nets. Hierarchical floorplanning blocks provide a means to rapidly create and arrange functional groups (clusters) of physical elements with respect to the circuit's architecture. Automatic generation of net topology, termination strategy, and power-density management accelerate floorplanning. On-line timing-path estimation guides users to an optimal arrangement that meets the design's timing, setup-and-hold time specifications.

Throughout the floorplanning session, real-time slack allocation is computed for all critical-timing paths *(Fig. 3)*. Information about the volume of connectivity between blocks, timing violations, space violations, and thermal problems are calculated and presented to users in real time. With every movement of floorplan blocks or components within a block, path timing budgets are redistributed using delay estimates based on detailed device, substrate-material, and interconnect physical models. Violation of setup-and-hold time specifications are displayed graphically and in tabular form.☐

PRICE AND AVAILABILITY

IS is available immediately on HP-700 Series and Sun workstations. Pricing for a fully-configured IS starts at $170,000. Base price of the IS floorplanner is $50,000. The IS synthesizer starts at $100,000. Interfaces for third-party front- and back-end environments cost $10,000 each.

Interconnectix Inc., 10220 S.W. Nimbus Ave., Bldg. K4, Portland, OR 97223; (503) 684-6641; fax (503) 639-3469. **CIRCLE 511**

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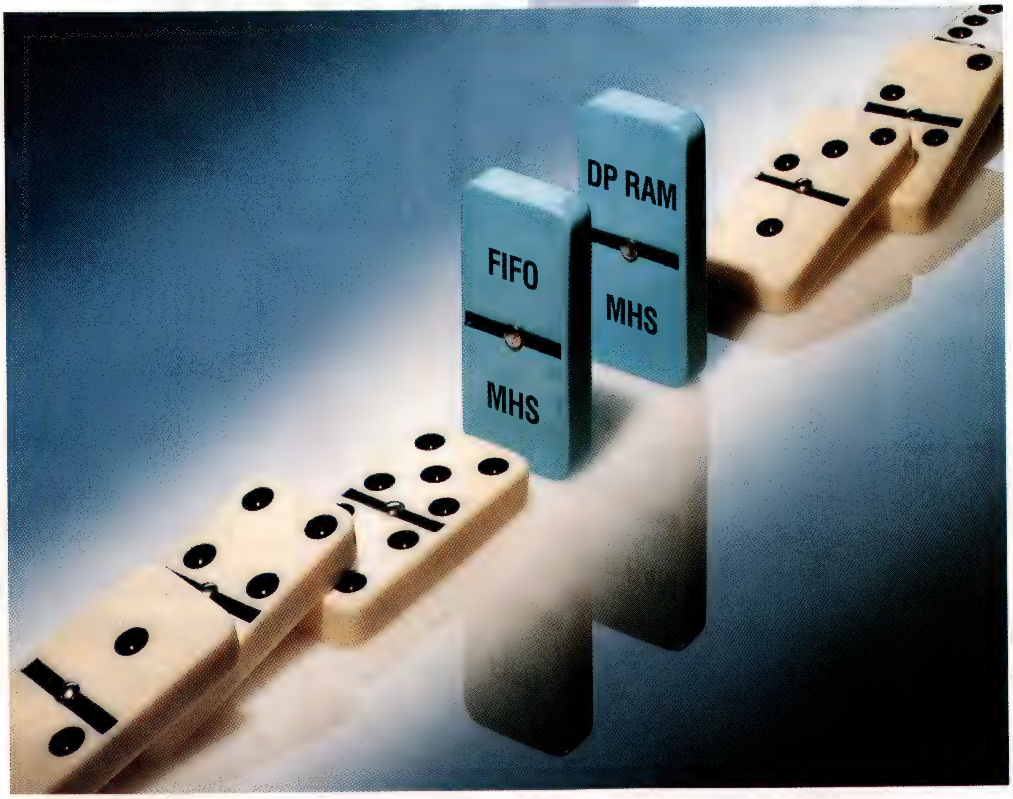

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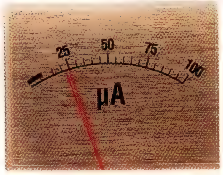

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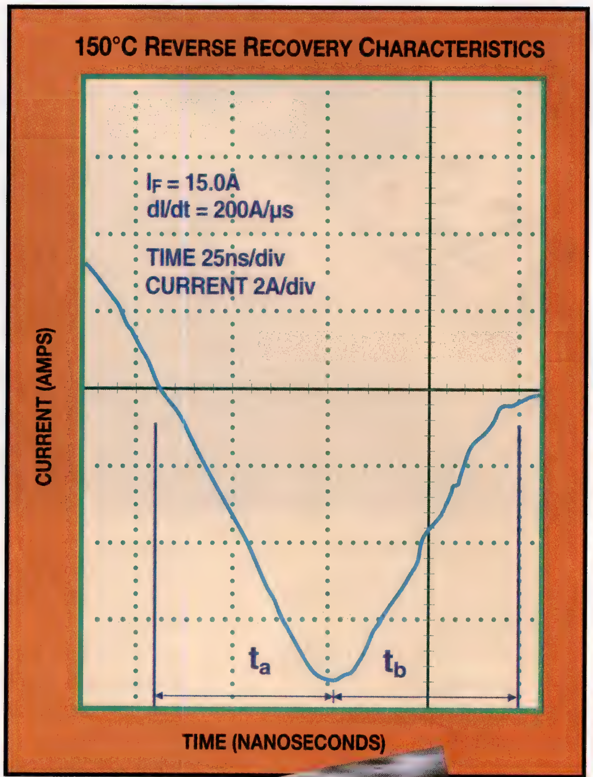

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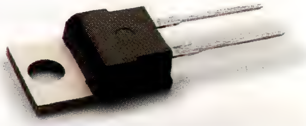

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THE PITFALLS OF SPEAKER SELECTION FOR MULTIMEDIA

DESIGNERS MUST DEAL WITH THE PROBLEMS OF VIBRATION AND THE MAGNETIC INTERACTIONS BETWEEN THE SPEAKERS AND OTHER SYSTEM COMPONENTS.

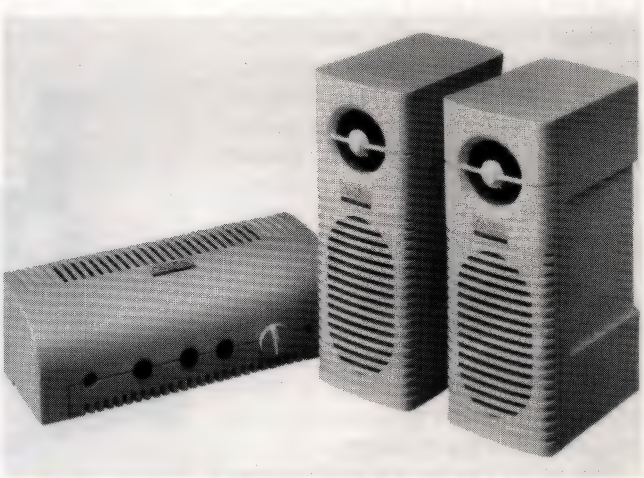
MICHAEL KLASCO
Menlo Scientific Ltd., 39 Menlo Pl.,
Berkeley, CA 94707; (510) 528-1277.

Multimedia has become a catch-all term for many emerging audio and video technologies. By definition, multimedia includes more than one media, perhaps containing audio and visual information, with the video component often including text and graphics. The audience can vary from an individual sitting in front of a computer monitor to a crowded auditorium with an HDTV video projection system.

One of the keys to the audio portion of a "personal-use" multimedia system is the design and specification of the sound-reproduction subsystem. Speaker selection may be done by the video-monitor designer (if the speakers are embedded into the monitor) or by the computer-case packaging engineer (when the speakers are part of an all-in-one multimedia system). The selection also may be done by system integrators or value-added-retailers who assemble multimedia packages. For retrofits, after-market outboard speaker systems, perhaps with built-in amplifiers, can be selected by end users and located near or attached to the monitor *(Fig. 1)*.

When selecting speakers for a television, table radio, or portable stereo, system designers typically will survey OEM speaker catalogs. In the catalogs, the speakers are categorized by speaker type, such as general purpose, magnetically shielded, high-fidelity consumer, commercial, industrial, and so forth. Unique multimedia speaker requirements have yet to be characterized and defined.

Aside from the magnetic-shielding arrangement that reduces the stray flux field from the speaker's magnet, the current crop of television loudspeakers are mostly generic general-purpose devices whose materials and designs reflect few of the speaker-technology advances made in the last decade. The present efforts of the OEMs manufacturing TV speakers are to reduce price and maintain direct



1. BECAUSE THEY'RE NOT PART **of the CPU or monitor subsystems, after-market speakers, such as Altec Lansing's ACS50, give users a great deal of freedom in placing the units for optimum stereo imaging.**

interchange compatibility with their competitor's products, rather than produce extended bass, cleaner sound, or wider dynamic range. But recent developments in speaker technology combined with rising end-user expectations will soon change the status quo. Video and computer system designers often view speaker selection as a generic process: Simply get the speaker that fits into the mounting location and turn the amplifier on. If sound comes out, go on to the next part of the project.

However, the combination of today's high customer expectations, stereo CD-ROM sound sources, and 16-bit CD-quality sound cards means the days of employing general-purpose speakers are over. While electrical engineers are well-versed in the criteria for selecting power supplies, CRTs, and other subsystems, speaker-transducer selection often has been a hit-or-miss process based on indifference, wisdom, or witchcraft.

Performance criteria listed in speaker-vendor catalogs typically includes sensitivity, resonance frequency, power handling, a response curve, and a mechanical drawing. Speaker sensitivity and impedance determine the amount of power that's needed to drive the speaker to an adequate listening level. If the amplifier doesn't supply enough power to drive the speaker, then it may be operated at clipping, leading to overheating and eventual failure.

Simply put, wide dynamic-range and bandwidth sound sources, such as CDs and sound-card synthesizers, encourage users to raise sound levels beyond what the designers had anticipated. If the sound is clean, then enthusiastic users tend to increase the level until the sound distorts. Hence, designing in a graceful overload, either by a limiter circuit or by simply not supplying enough gain for the system to reach a distortion level, is a good idea. Note that if the amplifier is being overdriven, the power supply, which is usually shared with the monitor or other components in an integrated multimedia product, also is in jeopardy of being overdriven.

This effect can have deleterious results on the operation of the system's remaining components. Remember that most switching power supplies start to lose the quality of their regulation when above half power. There's also another motivation for designing a "fail-safe" system that can't clip. Over-driven amplifiers flatten the waveform, resulting in square waves. The thermal duty cycle of a square wave is high, which can eventually burn out a speaker. While good design techniques are now common in most portable CD players, it's not always the case with some recent multimedia designs. Potential "short-cuts" often sabotage the benefits of 16-bit digital technology. These include amplifier input connections that are padded down and driven from the outputs of a lower-power amplifier, and audio op-amps driven in a single-ended configuration without adequate rail voltage for sufficient dynamic range to reproduce the audio without clipping.

Speaker sensitivity ranges from 80 dB at 1 W and 0.5 m for 1-in.-diameter speakers to 90 dB at 1 W and 0.5 m for 3-in.-diameter speakers (at 1 m, the level is 6 dB less). These sensitivities are in the range of only 1%. Listening levels at a distance of 18 in. will typically range from about 75 dB to over 95 dB. A headroom of 6 dB is desirable, making an amplifier power of 10 to 35 W per channel appropriate.

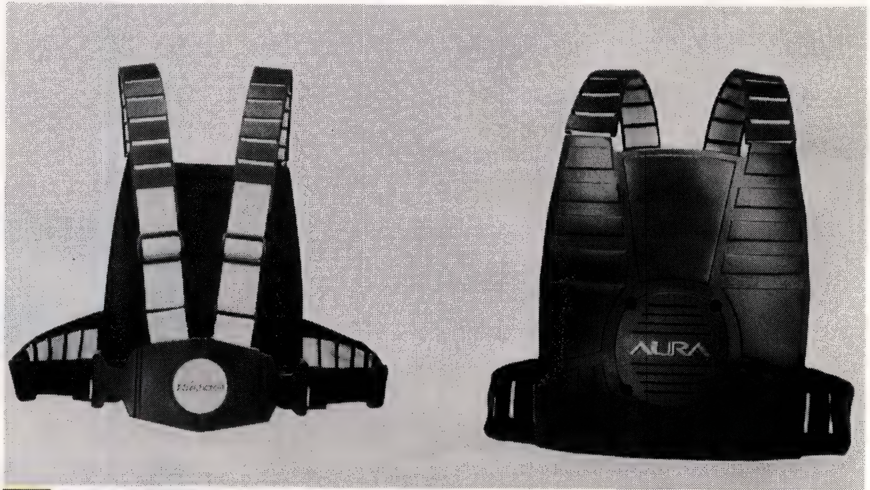
Techniques to increase speaker sensitivity include stronger magnetic systems, such as the new high-energy neodymium magnets; lower mass voice coils, such as aluminum or copper-clad aluminum wire voice coils instead of copper wire; and larger cones featuring new light-weight materials.

Impedance must also be considered—the lower the impedance, the more current the speaker will draw from the amplifier. Typical values range from 4 to 16 Ω, with piezoelectric elements offering somewhat higher values (but very limited bass response). High-impedance voice coils above 16 Ω may indicate the use of very-fine-gauge voice-coil wire, which is often accompanied by higher failure rates when overdriven. Fine wire is considered AWG (American Wire Gauge) 36 or higher.

As the wire's cross-sectional area decreases, so does the insulation thickness, mechanical strength, and current-carrying capacity. On the other hand, an increase in the number of wire turns in the magnetic gap increases the BL (motor strength). Because a thinner wire allows more wire in a given speaker magnetic-gap geometry, lower power handling and current consumption are traded off for a higher BL. A safe range for a multimedia speaker is from 30 to 34 AWG.

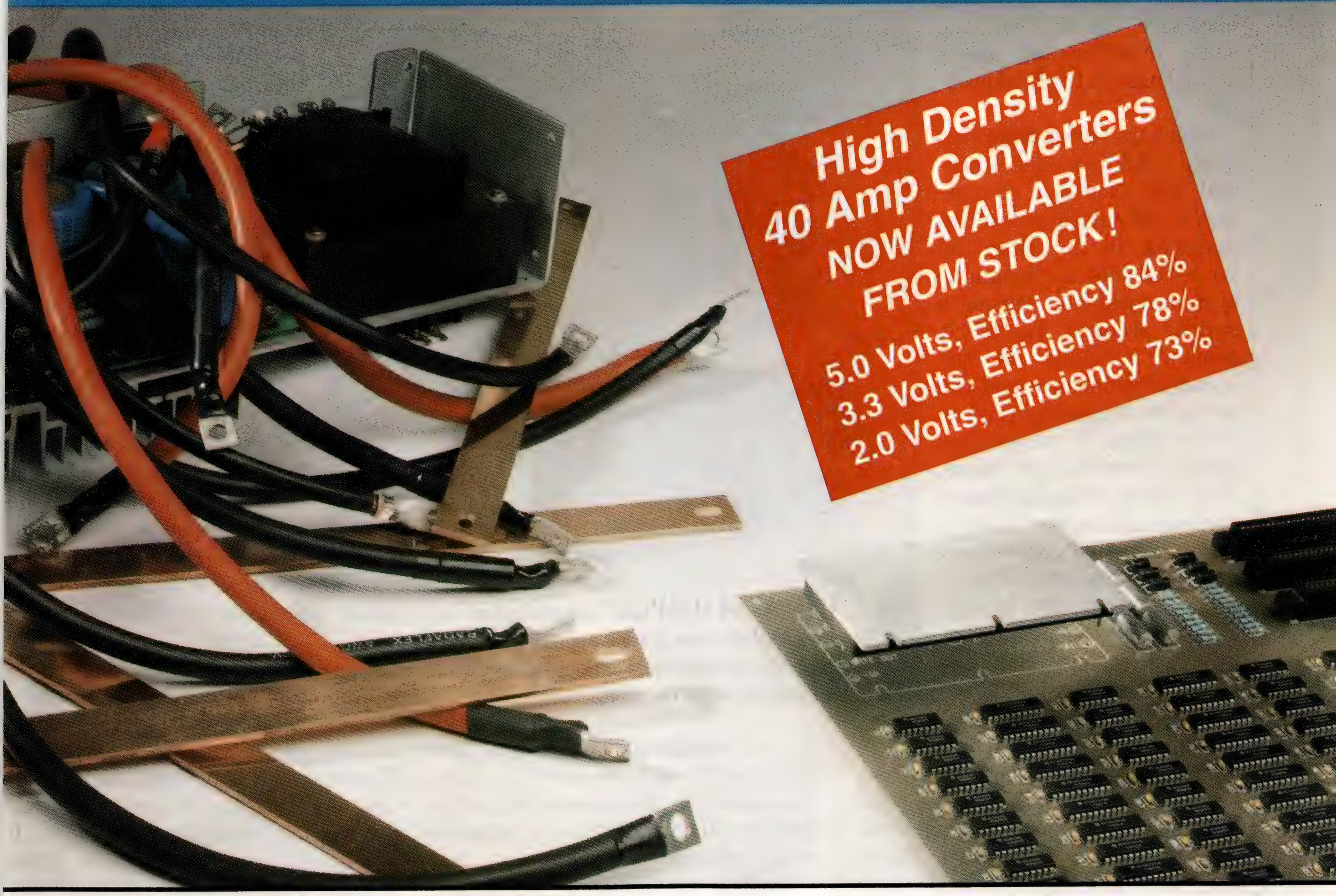
Speaker power-handling ratings can reflect two factors: onset of distortion or the power level at which the speaker may fail. It must be determined whether the speaker's usable output is sufficient for the intended application. Most important is to actually install the speaker within the product enclosure for testing.

The enclosure affects both the speaker's bass characteristic and the power handling. Designers must also look out for any annoying buzzes and rattles from other hardware within the product. Of course, the speaker must be evaluated not just within the



2. BASS VIBRATION IS SENSED through bone conduction rather than heard using the Bass Interactor. Developed by Aura Systems, this system eliminates interference with the CRT and disk drives.

ower Distribution vs. Distributed POWER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enclosure, but also with the same amplifier and power supply used in the final product.

Speakers suffer from two types of failure modes—thermal and excursion. Excursion is the culprit at low frequencies. In this case, the voice coil hits the magnetic system backplate, causing a serious problem. Therefore, proper matching of the speaker compliance and the enclosure volume is critical. For example, if the speaker isn't in its own sub-enclosure, then it's up to the speaker's suspension to control and restrict excessive cone movement. Conversely, when a small sub-enclosure is supplied within the monitor or product casing and the speaker's suspension is too stiff, the sound quality will be too thin and weak in the bass.

3. THE AV14 DISPLAY created by Apple uses a pair of upward-angled speakers to achieve optimal stereo imaging and improved voice intelligibility. For extended bass, a bass-reflex port is located in the rear of the casing.

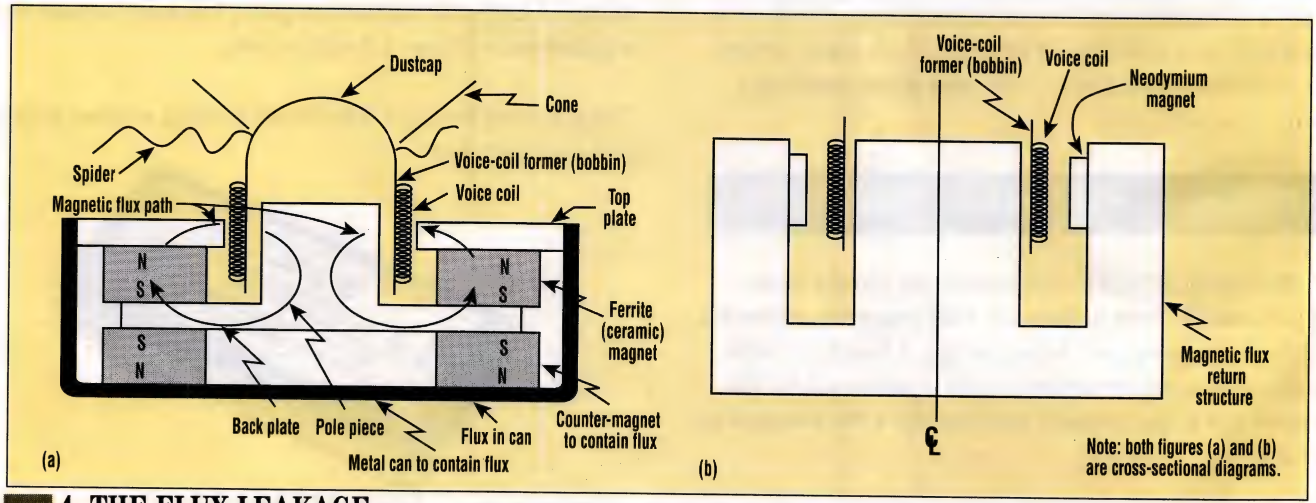
Thermal failure occurs from excessive heat buildup on the voice coil. One solution is to increase the thermal rating of the voice-coil bobbin. This is done by upgrading from kraft paper to Kapton polyimide film, using higher temperature adhesives, and selecting 150°C or 180°C rather than the more common 105°C- to 130°C-rated materials. Above 180°C, there are 200°C and 220°C voice-coil wires and adhesives. Overspecifying temperature ratings for voice-coil wire does have its own problems. These include poor wind quality and a required mechanical abrasive lead-out-wire insulation-stripping technique that can be somewhat awkward to apply.

Perhaps a better solution is to specify a speaker that operates cooler at a given output level. This is done by balancing good sensitivity and optimum materials. Black-caustic-etch zinc plating of the steel-magnet return structure is more effective at pulling heat off the voice coil than silver-zinc plating due to better heat emissivity. Dupont's Black Kapton MTB polyimide bobbin material is thermally conductive and also boasts high heat emissivity.

One of the most effective ways to prevent voice-coil burnout comes from Ferrofluidics Corp., Nashua, N.H., which offers ferrofluids, a thermally conductive magnetic fluid that's commonly used in audio high-fidelity and auto-sound speakers. The fluid, held in the magnetic gap by the intense flux field, offers four times less thermal resistance than the air it displaces. Ferrofluid transfers the heat from the voice coil to the magnetic system, where it's dissipated.

The cost of a failed speaker in the field and the return of computers or monitors due to failure is well beyond the cost savings of an inadequate speaker. Power ratings may range from a fraction of a watt for low-grade general-purpose devices to 20 or 30 W for hi-fi add-on multimedia speakers. Note that as power handling and deep bass capability is added, sensitivity will generally be lost, thus requiring bigger power supplies and amplifiers.

The resonance frequency, often specified as “f_0,” is the speaker's lowest resonance point when it's not loaded by an enclosure. If a design requires natural speech, then the


Dustcap
Cone
Spider
Magnetic flux path
Voice-coil former (bobbin)
Voice coil
Top plate
N
S
N
S
S
N
S
N
Ferrite (ceramic) magnet
Back plate
Pole piece
Flux in can
Counter-magnet to contain flux
Metal can to contain flux
(a)
(b)
Voice-coil former (bobbin)
Voice coil
Neodymium magnet
Magnetic flux return structure
℄
Note: both figures (a) and (b) are cross-sectional diagrams.

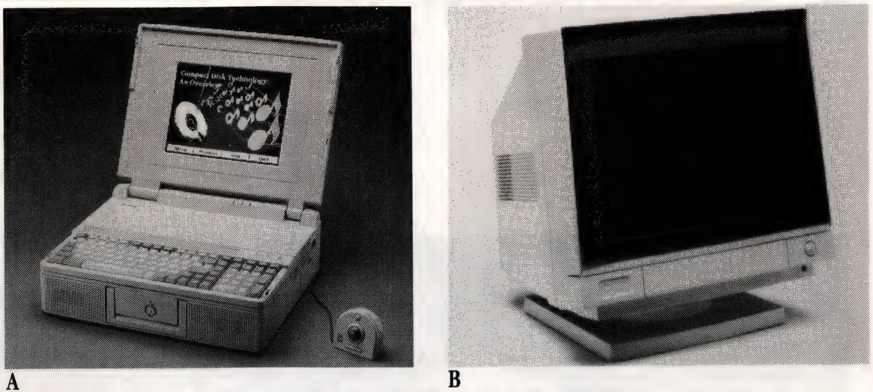
4. THE FLUX LEAKAGE in a conventional axial-ferrite shielded magnetic system can be reduced by placing a steel can over the countermagnet (a). The scheme is popular, but is bulky and increases the parts count. By enclosing a radial-oriented neodymium ring magnet in a magnetic return structure, there's an inherent shielding against stray flux (b).

speaker must have usable response to about 125 Hz (which essentially covers the fundamental pitch of male speech). If the speaker's fundamental resonance is above 200 Hz, it can't reproduce the fundamental resonance of human vocal chords. Listeners will hear virtual pitch, often described as "telephone speech," which may be intelligible but perceived as tinny.

While a 3-in. speaker engineered to reproduce sounds down to 100 Hz with a properly designed rear chamber and bass reflex venting can be impressive, the resulting vibration might produce problems. This includes blurring of text on a CRT, increasing the settling time (and overall access time) on a CD-ROM drive, or even causing erratic hard-disk operation. Bass reflex is the technique of utilizing the speaker's unused backwave by tuning the back chamber and a vent to put this energy into phase with the speaker's front radiation to extend and reinforce the bass frequencies. Some of the fancier add-on speakers offer an optional remote subwoofer system that extends the deep bass response without shaking up critical electronic components. Because bass wavelengths are large, about 10 ft. for 100 Hz, the listener doesn't notice that the sub-woofer isn't built into the system.

One unique solution to extend bass for multimedia systems was developed by Aura Systems, El Segundo, Calif. Its Bass Interactor, now available for OEMs, is a bass-vibration transducer that's either worn or sat on by the user *(Fig. 2)*. Deep bass, down to below 20 Hz, is felt, rather than heard. Because the bass vibration is localized to the user's body by bone conduction rather than transmitted though the air, the operation of the drives and CRT remains unaffected.

The Trinitron tube, devised by Sony Corp., is popular with OEM monitor manufacturers for its many visual attributes, but its unique shadow mask behind the tube's glass face is vulnerable to being excited by external vibration and sound. However, this condition only prevails on certain models. The black stripes on the tube's face are actually many fine wires hung from the top, with a single stabilizing wire toward the bottom third of the screen.



5. ONE INCREASINGLY POPULAR METHOD **is to integrate the speakers into the computer case. They're typically located on the front face, such as in Toshiba's T6600 series. This configuration avoids vibration pickup by the display (a). Another technique is to place the speaker inside the existing monitor housing, such as in the case of the Proton display (b). Here, the speakers face off to the sides rather than forward.**

When the CRT bulb picks up sound energy and rings, this interferes with the stability of the wires, causing a slight rippling effect on the screen. Careful case design, such as deep molded ribs or mechanical decoupling, is required to attain the best results. These anomalies are subtle and not noticeable in TV viewing situations. However, when a viewer is only 18 inches away from a computer monitor, this phenomena becomes apparent.

In Apple's multimedia monitor, these problems were avoided by mechanically decoupling the speaker subenclosure from the monitor's outer casing. Also, a bass reflex vent exits from the rear of the shell, away from the CRT face. The speakers are located directly below the CRT for best stereo imaging *(Fig. 3)*. IBM's multimedia monitor avoids vibration transmission to the CRT by locating the speakers in the swivel base, below the ball joint, where the vibration is decoupled from the upper casing and CRT.

An engineered multimedia package should be fully tested and compatible with itself, meaning that all of its components interact without any problems. A systems integrator assembling a multimedia system must not only avoid the vibration and magnetic problems, but also the pitfalls associated with the interactions between sound and graphics cards. Such problems occur between the audio beating of the sound-card clock and the video-amplifier frequency.

The speaker's frequency-response curve is often taken in an anechoic chamber, a room that's acoustically treated to remove all acoustical reflecting surfaces. The response curve plots the amplitude (in decibels) over the speaker's frequency range. The smoothness and octave-to-octave balance indicates the speaker's general sound (tonal) characteristic.

Unfortunately, when the speakers are installed within the video monitor or computer case, the response may be degraded. A good criteria is that the listener be in line-of-sight to the speakers. Poorly shielded speakers cause interference with the CRT's magnetic focusing system, which is most critical along the edge of the screen. Sadly, the best location for the speakers acoustically are along the sides or bottom edge of the CRT, and they're the worst for magnetic interference. Generally, the larger the CRT, the more vulnerable it is to this type of interference. While 14-in. VGA monitors have been the de facto standard, 15- and 17-in. monitors are now becoming common.

Shielded conventional ferrite-magnet speakers are built with a countermagnet and an outer steel can to reduce magnetic interference, but often this isn't enough to prevent visible interaction with the CRT. At the juncture of the can and the speaker basket, a side-lobe of stray flux is usually present, and this also is in close proximity to the most magnetically vulnerable portion of the CRT edge *(Fig. 4a)*.

To reduce magnetic interference with the CRT, television speakers are often recessed a few inches within a sound duct. The cabinets of most stereo televisions would reveal sound-chamber ducting that's both complex

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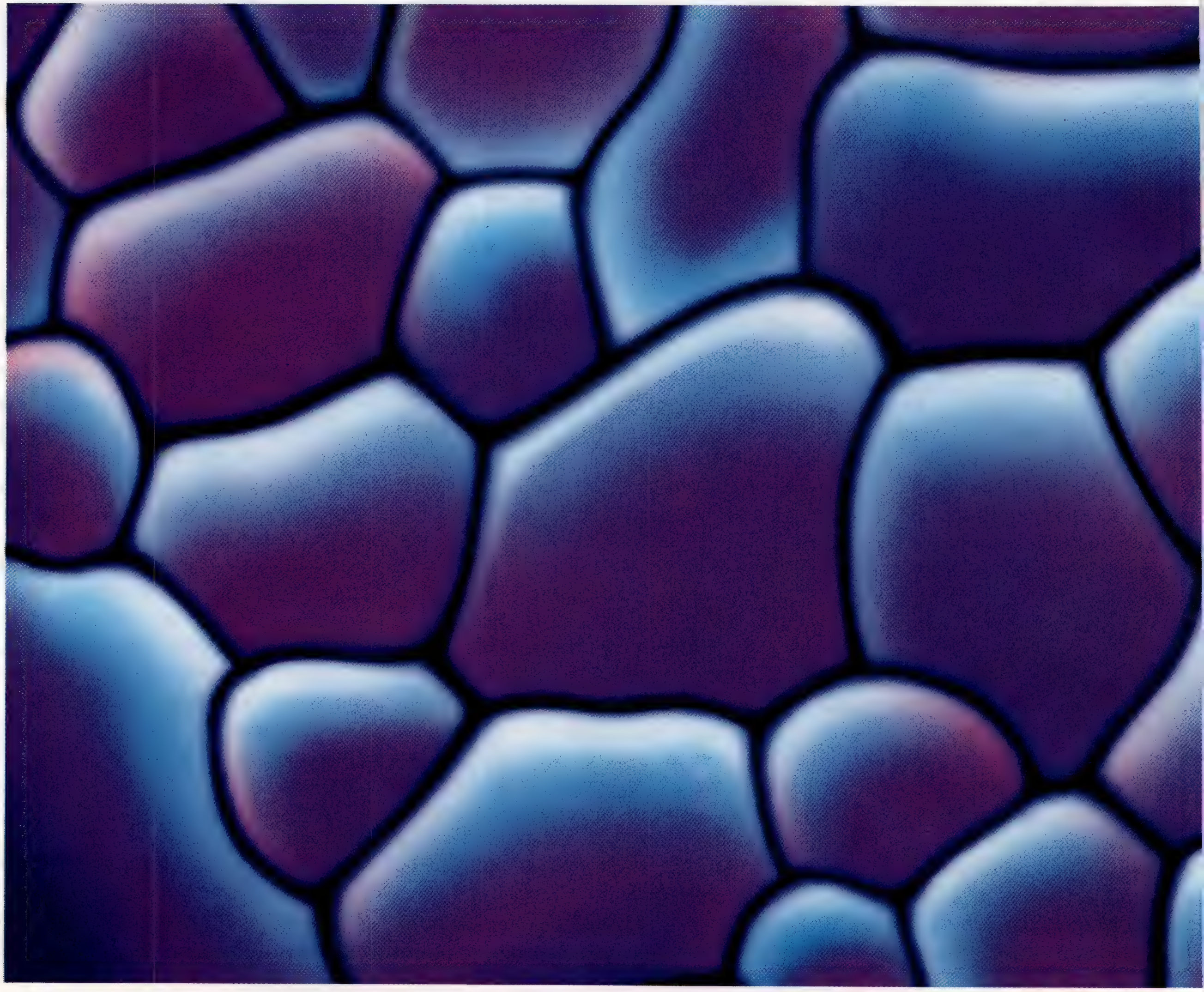

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to assemble and expensive to tool. Unlike horns or wave guides used in professional audio products, the type of ducting rarely follows good acoustic design practice and results in significantly degraded clarity, definition, and transient response.

One unique solution to the interference problem is the inherently shielded neodymium speakers developed by Aura Systems, which are currently employed by NEC, Daewoo, and a few Taiwanese multimedia OEMs. They're also used in audiophile and professional sound-quality speaker systems. Aura Systems holds patents on a unique magnetic structure that not only has less parts, less weight, and more energy than ordinary ferrite magnets, but also achieves much less stray magnetic field than even a conventionally shielded speaker *(Fig. 4b)*.

Other features of this new magnetic technology have contributed to the development of extended-range speakers that don't require separate tweeters or crossover networks. A hidden cost savings of this technology is that the stray flux field is virtually nonexistent. Hence, the speaker can be mounted to the front panel of even the most magnetically sensitive large-screen direct-view television or computer monitor without the usual sound-muffling duct baffles.

It's important to note that good stereo imaging also requires careful speaker placement. If the speakers are too far apart, then the sound source won't be solid, creating a hole-in-the-middle effect. If the speakers are too close together, then the spatiality and stereo image will be lost. Roughly, an equilateral triangle between the speakers and the listener is about right, ideally with the speakers toeing in (and facing upward, if they're mounted below ear level) toward the listener.

Three configurations for speaker location are becoming popular. The first is to build the speakers into the monitor; the second is to integrate them into the computer case; and, finally, outboard speakers, within their own enclosures, are popular as a retro-fit solution *(Figs. 5a and 5b)*.

Although many of the solutions discussed are appropriate for TV speakers, they simply won't work for video monitors. For example, if the speakers are located off to the sides of the monitor, then the TV viewer will still hear some direct sound, because the viewer is typically 5 ft. or more from the set. But the multimedia viewer is directly in front of the CRT. The sound heard from sideways-facing speakers mounted into the sides of the monitor will consist entirely of room reflections, making intelligibility poor.

Speakers and power amplifiers integrated into the computer case are becoming available from a number of case suppliers. Typically, the speakers are located on the front face of both portable and desktop computers (such as in Toshiba's 6400 and 6600). While placing the speakers neatly in the case avoids vibration pickup by the monitor, power-supply interactions between the audio amplifier and computer must be considered, as well as vibration from the speakers interfering with the access times of magnetic and optical disk drives. The case also must be located in such a position to produce a satisfactory stereo image (goodbye tower configurations!). Generally, the viewer will be facing the monitor, and the sound from case speakers will be a little low. A case design that allows the speakers to be angled would also be beneficial.

Although the basics of multimedia speaker design have been covered, endless refinements are necessary. Rising expectations in the multimedia market will further complicate audio vibration engineering requirements. Also, desktop video conferencing, which introduces a microphone into the video monitor, brings the problem of acoustic feedback between the microphone and speakers, as well as noise pickup problems from the cooling fan and hard-drive bearing. ☐

Thanks to Rob Baum, senior designer at Menlo Scientific, for his contribution to this article.

Mike Klasco, a principle of Menlo Scientific Ltd., an audio engineering consulting firm in Berkeley California, holds a BS degree in music, business, and technology from the School of Education at New York University.

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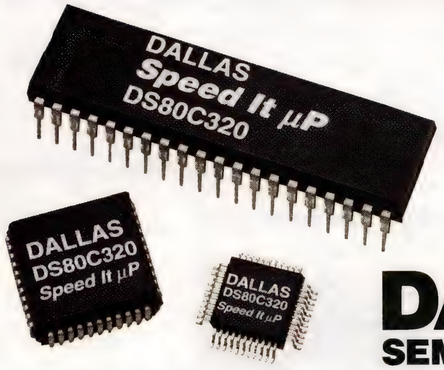

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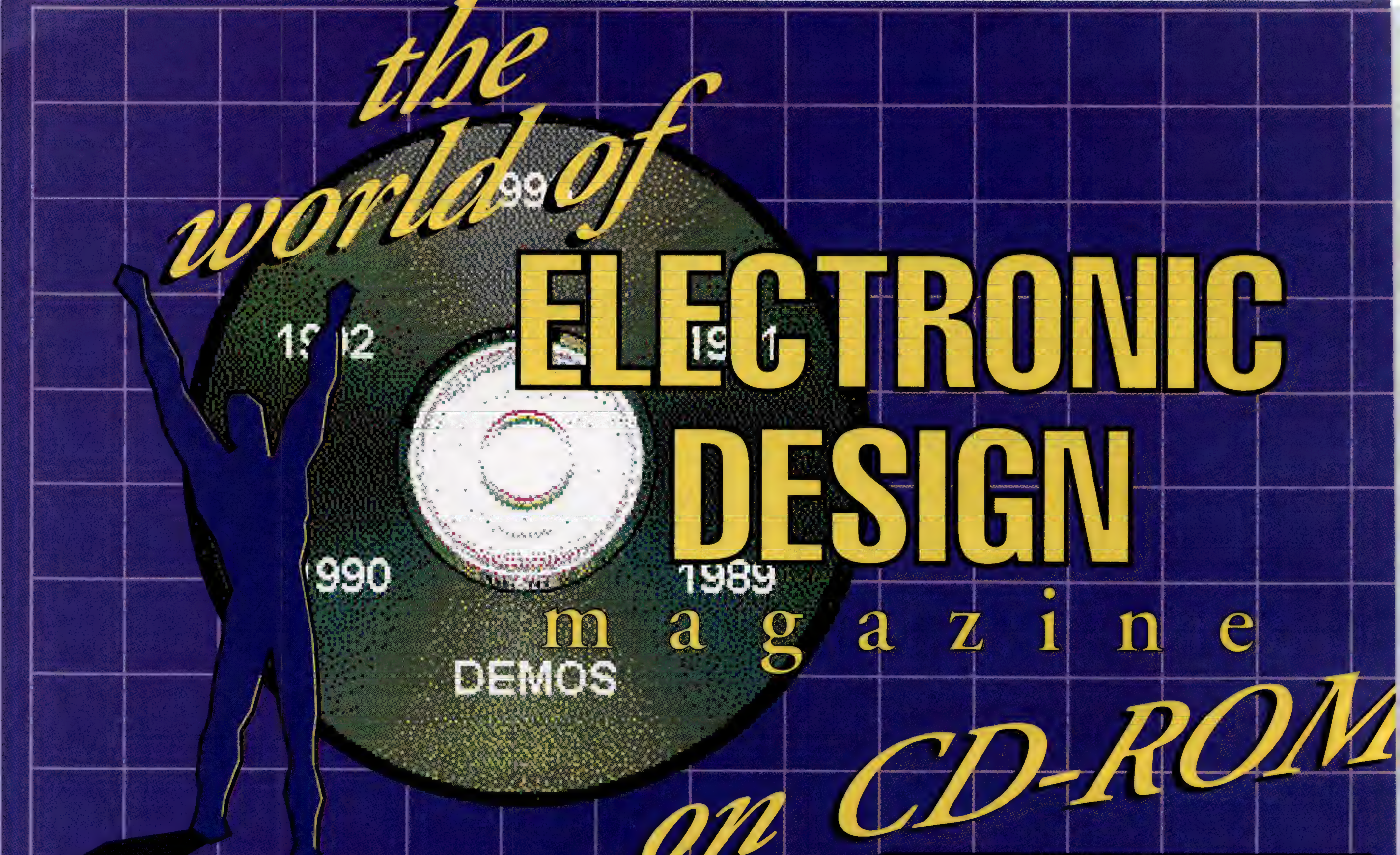

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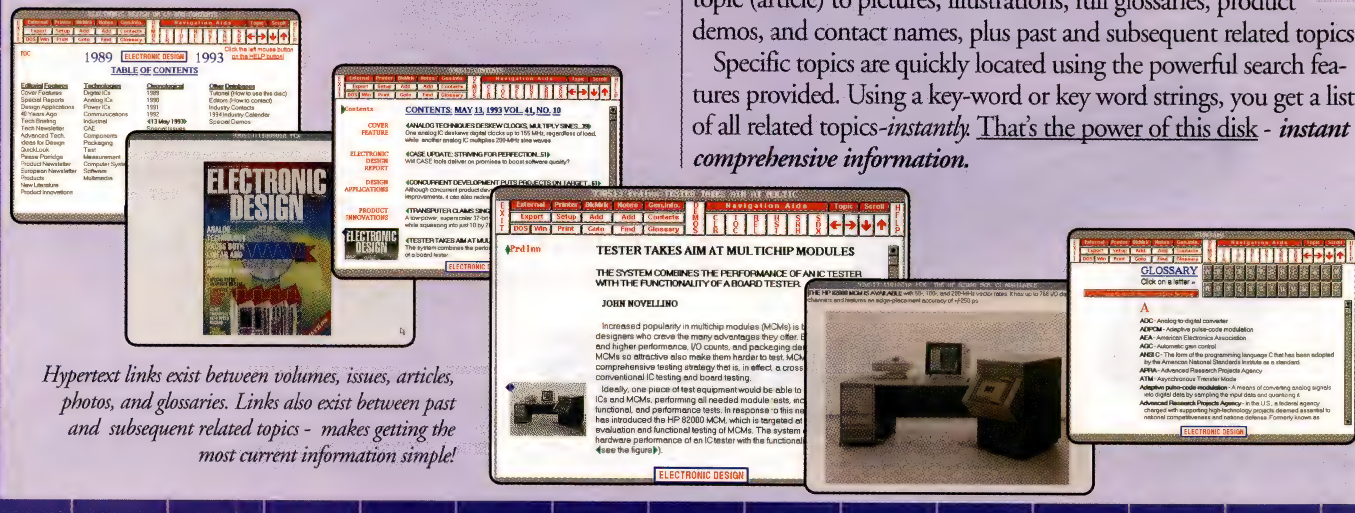

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TESTER TAKES AIM AT MULTICHIP MODULES

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JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is b designers who crave the many advantages they offer. E and higher performance, I/O counts, and packaging de MCMs so attractive also make them harder to test. MCM comprehensive testing strategy that is, in effect, a cross conventional IC testing and board testing.

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GLOSSARY

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A

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ADPCM - Adaptive pulse-code modulation
AEA - American Electronics Association
AGC - Automatic gain control
ANSI C - The form of the programming language C that has been adopted by the American National Standards Institute as a standard.
APRA - Advanced Research Projects Agency
ATM - Asynchronous Transfer Mode
Adaptive pulse-code modulation - A means of converting analog signals into digital data by sampling the input data and quantizing it
Advanced Research Projects Agency - In the U.S., a federal agency charged with supporting high-technology projects deemed essential to national competitiveness and nationa defense. Formerly known as

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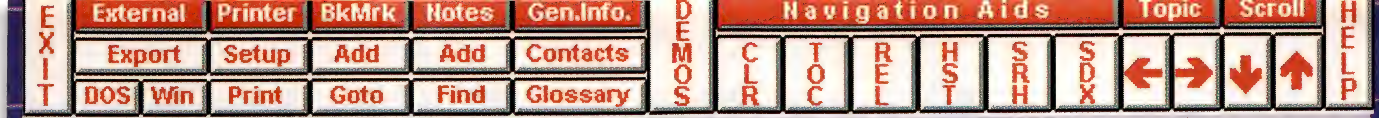

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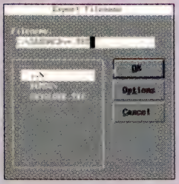

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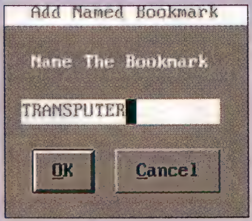
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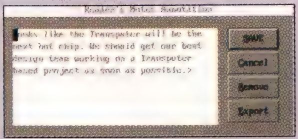

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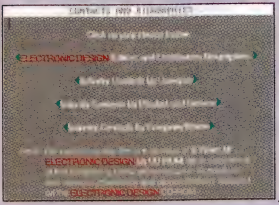

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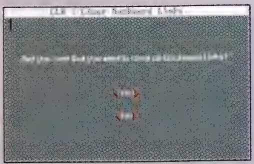

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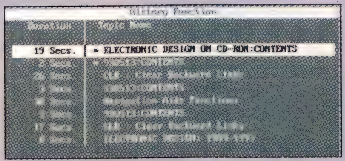
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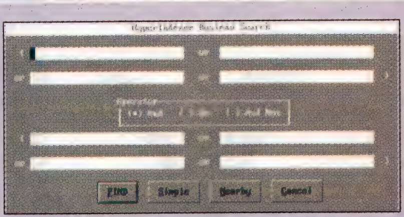

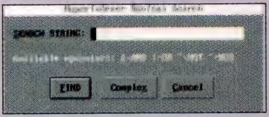

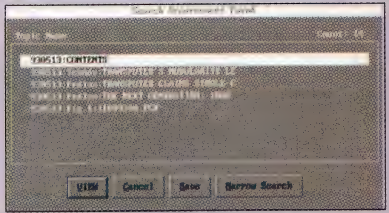

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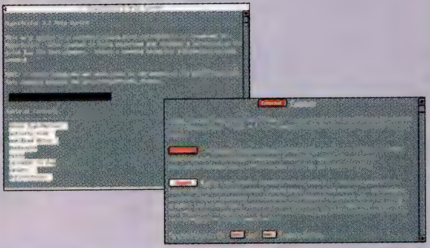

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BUILD IF/AGC AMP WITH FOUR PARTS

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An IF/AGC amplifier that features an 82-dB AGC range can be built using just four active components *(see the figure)*. It uses a simple two-transistor peak detector (the transistors, 2N3904 and 2N3906, are commonly available and low cost).

The peak detector consists of Q2, a temperature-dependent current source, and Q1, a half-wave detector. Q2 is biased for a collector current of 300 μA at 27°C; the temperature coefficient is 1 μA/°C.

The current into capacitor C_{AV} is the difference between the collector currents of Q2 and Q1, which is proportional to the output signal's amplitude. The automatic gain control voltage, V_{AGC}, is the time integral of the error current.

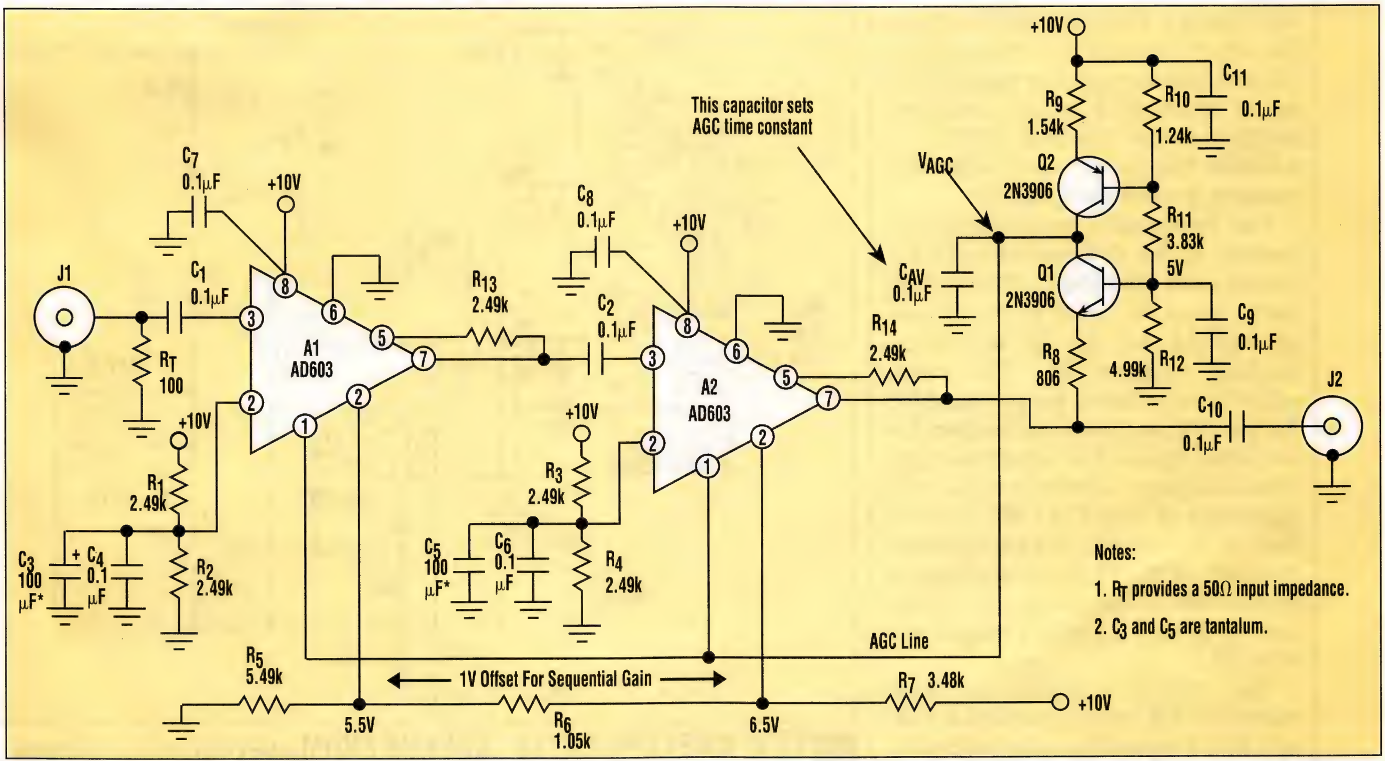
For V_{AGC} (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small, V_{AGC} will increase. This in turn causes the gain to increase until Q1 conducts and the current through Q1 balances the current through Q2.

To illustrate further, first consider the case when R_8 is zero and the output voltage V_{out} is a squarewave at, say, 455 kHz (which means it's well above the corner frequency of the control loop). During the time V_{out} is negative with respect to the base voltage of Q1, Q1 will conduct. When V_{out} is positive, Q1 cuts off. Because the average collector current of Q1 is forced to be 300 μA and the squarewave has a duty cycle of 1:1, Q1's collector current when conducting must be 600 μA.

Because Q1's average emitter current is 600 μA during each half-cycle of the squarewave, a resistor of 833 Ω would add a PTAT (proportional to absolute temperature) voltage of 500 mV at 300 k, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used, and to a lesser extent, on the waveform that optimizes the temperature stability. For the 2N3904/3906 pair and sinewave signals, the recommended value is 806 Ω.

The 1.8-kHz low-pass filter which R_8 forms with C_2 reduces distortion due to ripple in V_{AGC}. The output amplitude under sinewave conditions will be higher than for a squarewave, since the average value of the current for an ideal rectifier would be 0.637 times as large. As a result, the output amplitude would be 1.88 (= 1.2/0.637) V, or 1.33 V rms. In practice, the somewhat non-ideal rectifier result in the sinewave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The entire circuit operates from a single 10-V supply. Resistors R_1, R_2, R_3, R_4 bias the common pins of A1 and A2 at 5 V. This pin is a low-impedance point and must have a low-impedance path to ground. In the cir-



Notes:

1. R_T provides a 50Ω input impedance.
2. C_3 and C_5 are tantalum.

JUST FOUR ACTIVE COMPONENTS are used in this configuration that provides 82 dB of AGC. Q1 and Q2 form a temperature-compensated peak detector that holds the output at 1.4 V rms for inputs as low as −67 dBm (100 μV rms) to +15 dBm (1.4 V rms).

cuit shown, it's provided by the 100-μF tantalum capacitors and the 0.1-μF ceramic capacitors.

The gain of A1 and A2 is set at 42 dB for an overall gain of 84 dB. They operate in sequential gain, which means that the gain of A1 goes from minimum to maximum and then A2's gain does the same. This is beneficial because first, the signal-to-noise ratio is at its maximum for as long as possible, and second, the signal strength in dBm can be determined from the AGC voltage (the gain changes at 40 dB/V). The gain is 0 dB for $V_{AGC} \approx 5$ V, and 82 dB for $V_{AGC} \approx 7$ V. In the circuit, the gain-control offset voltage between pins 2 (GNEG) of A1 and A2 is 1.05 V (42.14 dB × 25 mV/dB), which is provided by a voltage divider consisting of R_5, R_6, and R_7.

The circuit's bandwidth exceeds 40 MHz and can be used at any of the standard IFs (such as 455 kHz, 10.7 MHz, or 21.4 MHz) within this range. At 10.7 MHz, the AGC threshold is 100 μV rms (–67 dBm) and its maximum gain is 83 dB (20 log 1.4 V/100 μV). The circuit holds its output at 1.4 V rms (3.9 V p-p) for inputs as low as –67 dBm to as high as +15 dBm (82 dB), where the input signal overdrives the amplifiers. For a –30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental and the third harmonic is 35 dB down.☐

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

IFD WINNER

IFD Winner for February 21, 1994

Clive Bolton, Bolton Engineering Inc., 37 Washington Street, Melrose, MA 02176. His idea: *"Telephone Ring Generator."*

CIRCLE

522

RMS CONVERTER HAS EXCELLENT CMR

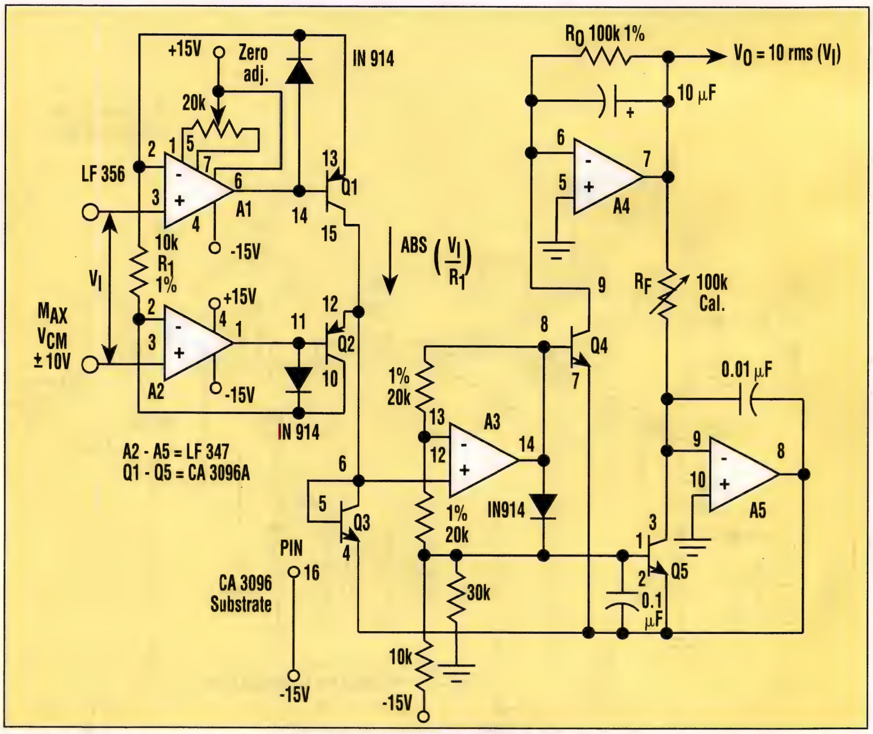
W. STEPHEN WOODWARD and JOHN PETERSON
Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290.

Designs for rms converters are common, particularly the single-chip monolithic solutions. This circuit *(see the figure),* however, differs from the others because of its versatile instrumentation-amplifier-type differential inputs that feature excellent common-mode rejection (CMR). In addition, the circuit is built with inexpensive, generic components.

The first step in input-signal processing is the differential-input absolute-value circuit (ELECTRONIC DESIGN, *April 16, 1992, p. 93).* It consists of A1, A2, Q1, Q2, and input-scaling resistor R_1. The zero-adjustment trimmer pot provided for A1 permits accurate calibration for low-level inputs. The absolute-value circuit displays a common-mode voltage range of ±10 V, a CMR equal to that of A1 and A2, and an input impedance of $\approx 10^{12}$ Ω. It produces a current-mode output at the collectors of Q1 and Q2 with a magnitude of V_I/R_1.

This current is applied to diode-connected Q3, which produces a voltage that's logarithmically related to $\text{abs}(V_I/R_1)$ as the first stage of signal processing in the rms computing circuit. The rms computation is performed by a variation of the so-called "implicit" method. The log signal produced by Q3 is doubled by A3 and then applied to antilog transistor Q4. Because $\text{antilog}(2 \log(x)) = x^2$, the collector current of Q4 (I_{Q4}) is proportional to the instantaneous square of Q3's collector current. I_{Q4} is averaged and converted to output voltage V_O by A4.

Amplifier A5 and transistor Q5 produce a signal related to $\log(V_O)$, which is applied to the emitters of Q3



THIS RMS CONVERTER DIFFERS FROM other designs because it includes instrumentation-amplifier-type differential inputs. The inputs offer excellent common-mode rejection.

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and Q5. This effectively subtracts it from the V_{BE} of Q3 and adds it to the V_{BE} applied to Q4. Due to the relationship of addition and subtraction of logarithms to multiplication and division, the net result of this $\log(V_O)$ feedback is that I_{Q4} is proportional to V_I^2/V_O. Because $V_O = \text{avg}(I_{Q4}R_O)$, $V_O = \text{avg}(kV_I^2/V_O)$, $V_O^2 = k\ \text{avg}(V_I^2)$, and $V_O = K\ \text{rms}(V_I)$. K and k are appropriate constants.

The scale factor of the rms conversion, K, is given by $(R_F R_O)^{1/2}/R_1$. In the example circuit, the scale factor equals 10. Thus, a differential input signal of 1 V_{rms} produces a V_O of 10 V.

Circuit frequency response includes both dc and those ac components with frequencies both well above the $R_O C_{avg}$ output time constant ($<<$ 10 Hz in the example), and below the slew rate and gain-bandwidth limitations of amplifiers A1 and A2 ($>$300 kHz for −3 dB in the example).

Within this range, circuit linearity is better than 1%. "Crest factor" capability is good due to the lack of voltage compliance limitations in the rms computation loop.☐

CIRCLE

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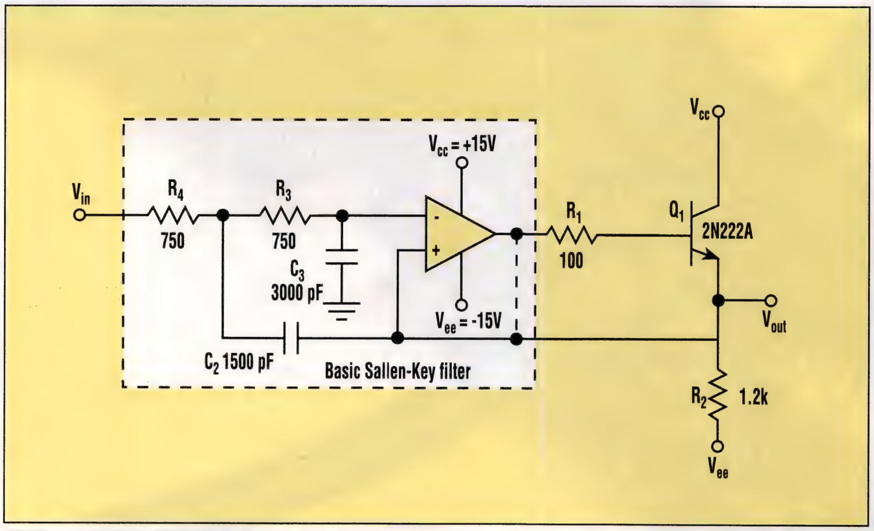
FILTER IMPROVES STOP-BAND REJECTION

MICHAEL A. WYATT

Honeywell Inc., 13350 U.S. Hwy. 19, MS-931-4, Clearwater, FL 34624.



1. WHEN FREQUENCY increases in the basic Sallen-Key low-pass filter, capacitor C_2 (in the feedback loop shown with the dashed line) and input resistor R_4 form a voltage divider with the op amp's output impedance. That ratio constitutes the filter's stop-band rejection. By adding an emitter follower (Q1) in the feedback look, amplifier output impedance can be reduced, improving the stop-band rejection.

Most op amps have a low output impedance at frequencies well below their closed-loop bandwidth, but as frequency increases, so does the output impedance. When the op amp is used in a Sallen-Key low-pass filter, this increase in output impedance can reduce the filter's stop-band rejection.

However, a simple emitter-follower buffer amplifier at the op amp's output can reduce the effects of the higher output impedance and improve the stop-band rejection.

The effect of increased output impedance can be seen in the basic Sallen-Key low-pass filter (including the dashed line for feedback in *Fig. 1)*. When frequency increases, capacitor C_2 (connected between the input and output) along with input resistor R_4 form a voltage divider with the op amp's output impedance. This division ratio is the stop-band rejection of the filter, and the higher the output impedance, the lower the stop-band rejection.

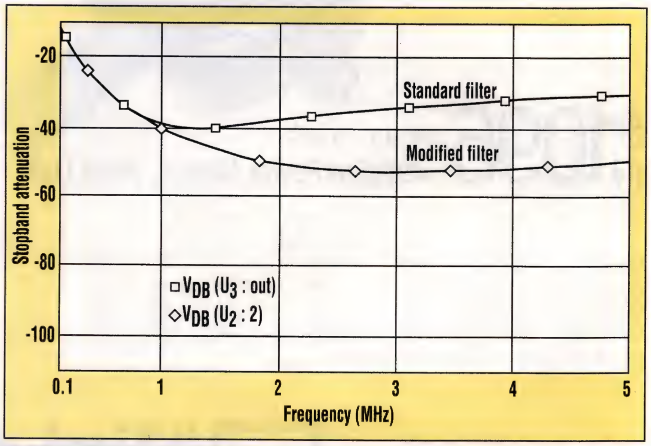
Stop-band rejection can be improved by breaking the feedback loop and adding a buffer amplifier, which lowers the amplifier's output impedance. Transistor Q1 and resistors R_1 and R_2 form an emitter follower that buffers the op amp output and provides a low output impedance beyond the bandwidth of the op amp. Because transistor Q1 is inside the feedback loop, degradation in the filter dc and pass-band response are avoided.

Spice simulations indicate a 20-dB improvement in stop-band rejection for the filter *(Fig. 2)*.☐

IFD WINNER

IFD Winner for March 7, 1994

Dan Retzinger, 17113 Baltar Street, Van Nuys, CA 91406. His idea: *"Build Efficient DC Lamp Dimmer."*



2. STOP-BAND rejection is improved by 20 dB, as indicated by the Spice simulation, which agrees closely with test measurements.

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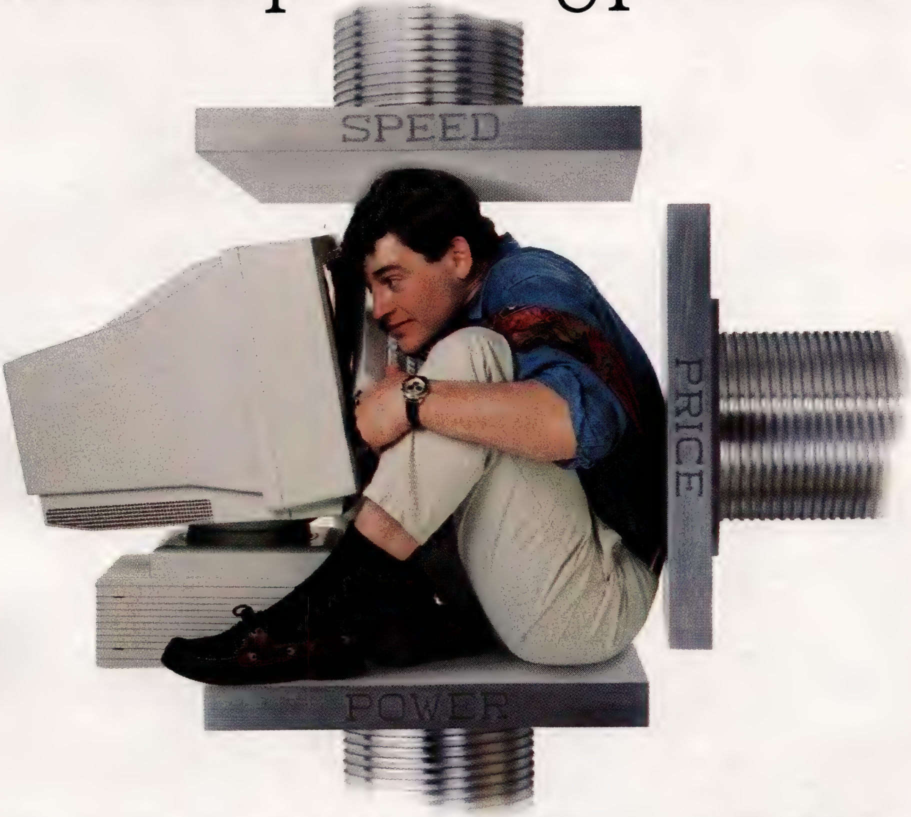

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Peaking, G=+2, (dB/MHz)	.1/100	.2/25	.12/75	.2/100
Slew Rate (V/μsec)	1200	1500	1100	2100
Diff Gain/Phase (%/°)	.01/.025	.02/.025	.02/.02	.12/.05
Supply Current (mA, Max)	5.5	6.7	6	4.5

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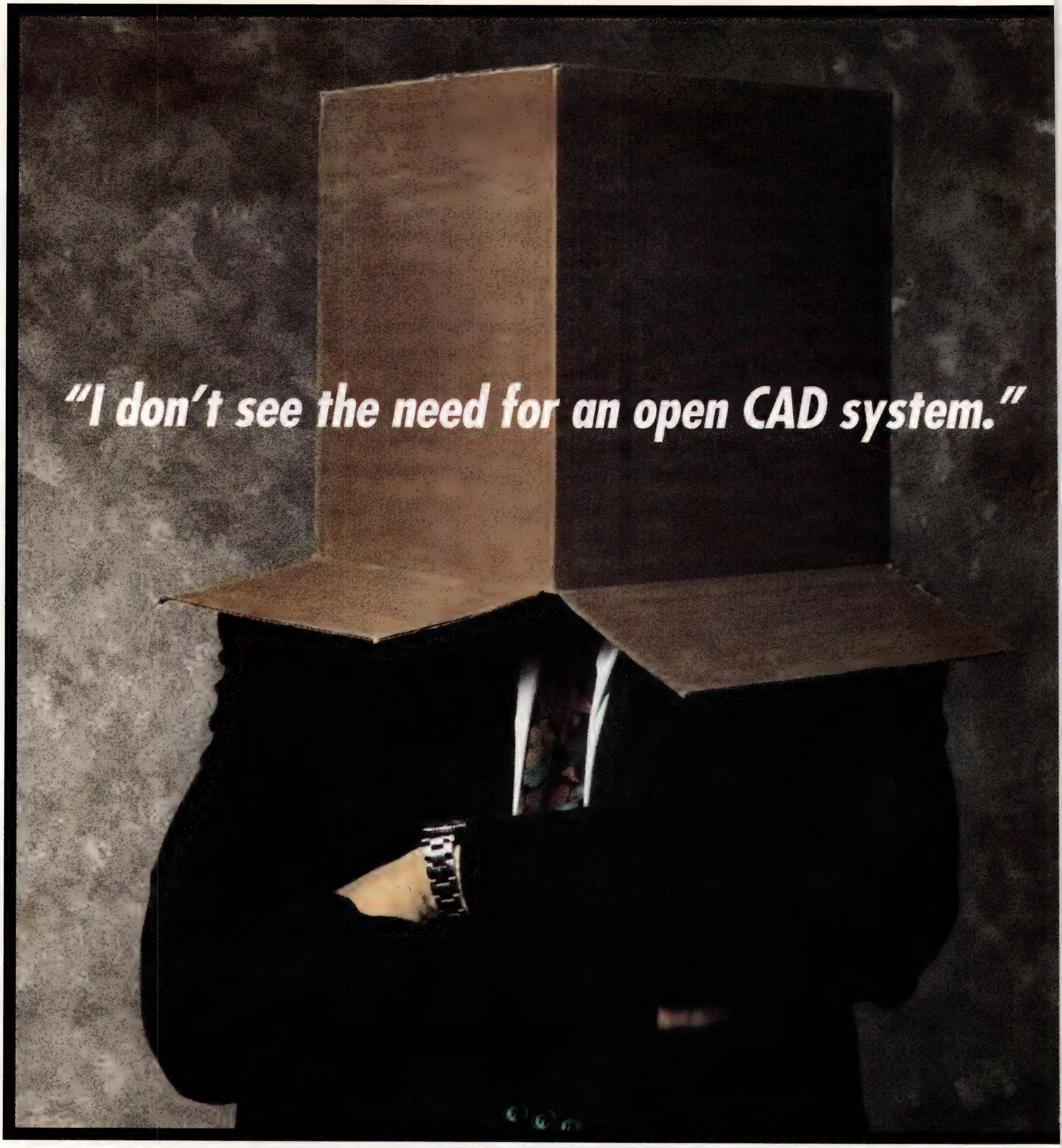
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ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

The U. S. data compression market, propelled by motion video, is expected to grow more than sixfold between 1993 and 1999, increasing from $101 million last year to about $667 million in 1999. That's the prediction of market researcher Frost & Sullivan. Data compression plays a key role in videoconferencing, digital television, electronic identification systems, desktop publishing, digital cellular, and digital answering machines, according to a recent report from the the Mountain View, Calif., company.

Data compression is becoming increasingly important because it reduces the need for storage and speeds transmission time for applications like video and imaging. The still image/text compression segment will be driven by identification systems, desktop and electronic publishing, and medical applications. Speech compression products will find application in digital answering machines, digital cellular phones, voice mail systems, and secure telephones. Competition is intensifying, with companies entering the market to capitalize on increasing demand; prices are expected to fall, and slimmer profit margins lie ahead, predicts Frost & Sullivan.

HEALTHY GROWTH FOR DATA COMPRESSION PRODUCTS (U.S.)

Year	Thousands of units	Revenues ($ million)
1993	3,367	101
1994	5,451	162
1995	9,099	257
1996	14,478	378
1997	20,924	500
1998	27,408	600
1999	32,793	666

Source: Frost & Sullivan Inc.

TALES FROM A SKUNK WORKS

We've been talking about how incredibly difficult it is to move to better paradigms for product development. Even when their very survival is at stake, most Western corporations resist the shift so strongly that it is easier to go with the flow than to attempt change.

I want to devote this column to a courageous and dedicated colleague who devoted his life's service to improving the world. He was a hero and a messiah to our trading partners, but died a prophet without honor in his own land: Dr. W. Edwards Deming.

I speak with many who turned off about teams after being ground up by the quality process, and I deplore the bureaucrats who waste millions and destroy innovation in the name of quality. Some are surprised that I admire Deming, but I do. I respect Deming because of his integrity, dedication, and focus on results. The most innovative devices are worthless unless one can become the high quality, low cost producer. The output of the skunk works I am describing can easily feed into Deming's quality programs.

> "The trouble with Total Quality Management is that there is no such thing. It is a buzzword. I have never used the term, as it carries no meaning."
>
> W. Edwards Deming, 1993.

Deming deserves much of the credit for transforming Japan from a shattered nation into the world's most effective techno-industrial society. The Japanese cherish the Deming Prize for corporate quality, which was established in 1951. He was their mentor, their great American *sensei*.

Deming could have enjoyed a pleasant retirement, but he devoted the last decades of his life "trying to keep his country from committing suicide." He noted the same trends that I discuss—the U. S. decline in building products and of our prosperity.

We were not very receptive to his teachings, preferring process pabulum to mutual trust, continuous improvement, statistics, and close relationships with suppliers and customers. Deming didn't get his first major U. S. client until 1979. In later years, he grew increasingly frustrated, saying, "I'm desperate. There is not enough time left."

By 1993 Deming was plagued by phlebitis, prostate cancer, and almost total hearing loss, but he kept trying. In his last year, at the age of 93, he gave 30 four-day seminars. His last was from a wheelchair, linked to an oxygen tank, a few weeks before his death.

I give seminars too, and I shudder at the thought of such a grueling schedule. Deming didn't need the money or the recognition; he did it because he cared. He gave us his all. Dr. Deming, we will miss you. We can re-learn product development, from innovation to implementation, and you helped. Thank you.

John D. Trudel, CMC, lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk*. To order, phone (503) 280-8547.*

EYE ON ISO 9000

Valor Electronics Inc., a subsidiary of GTI Corp., a supplier of signal processing and power products such as pulse transformers, filters, modules, and DC/DC converters, has been awarded ISO 9001 for its San Diego headquarters and ISO 9002 for its Hong Kong production facility. Contact Valor Electronics, 9715 Business Pk Ave., San Diego, CA 92131-1642; (619) 537-2500. CIRCLE 460

Equipto Electronics Corp. has received ISO 9002 certification for the manufacturing quality of standard modified and custom modular electronic cabinets, computer furniture, and workstations. For a free copy of the company's catalog or a demo disk (PC software, CAB-NET) contact Equipto Electronics Corp., 351 Woodlawn Ave., Aurora, IL 60506-9988; (708) 897-4691; fax -5314. CIRCLE 461

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Excelsior Manufacturing, a contract manufacturer specializing in printed-circuit boards with surface-mounting technology, has been registered to ISO 9002. Contact Excelsior, 1980 Concourse Dr., San Jose, CA 95131; (408) 944-9060; fax -8063. CIRCLE 464

OCG Microelectronic Materials Inc.'s European headquarters in Awijndrecht, Belgium, has been registered as complying with ISO 9002 for an ultraclean production plant for metal ion-free positive resist developers and ancillary products, photosensitive and nonphotosensitive polymides. For further information, contact OCG Microelectronic Materials Inc., 3 Garret Mountain Plaza, West Paterson, NJ 07474; (201) 977-6036.

CIRCLE 465

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

The project manager maintains responsibility for the concurrent, cross-functional, management of the project. In this environment, this individual works to achieve an effective balance between development cost, product performance, product cost, as well as time-to-market objectives. Of the four parameters, product cost and performance are mostly determined by the architecture selected for the product. Likewise, this architecture significantly influences development cost by establishing the number of person months of effort that must go into product development to realize performance and cost objectives. Thus, the project manager determines how the work that must go into the realization of the product becomes distributed over time. Under these conditions, the application of resources to the project sets time to market.

To produce a project database, the project manager takes input supplied by management (usually in the form of directives and strong suggestions), knowledge of resources available to the project, and team networks—generated using the six-step method—to produce the plan for realization of the new product. Viewed from this perspective, you can see the contribution the team makes to the overall planning process. Team members provide the project manager with accurate data that makes it possible for him/her to effectively allocate resources to the effort.

The project manager manages the project's database and thereby the project. Creation and maintenance of the database improves the decision-making process of the project manager and others associated with the project. This common database produces the reports and charts used to lead, guide, and direct the project on a day-to-day basis. The table summarizes project management roles and responsibilities during the planning phase:

Methods:	Cross-functional, concurrent, "to do" list, project management
Tools:	Project database
Input:	Resource allocation to project Team networks Management information
Output:	Resource allocation to task Individual "to do" lists Project "to do" list Project Kmet chart Resource histograms Corporate milestone reference

Input items effectively manipulated by the project manager, produce the project database. Once in existence, database information and support tools produce the listed output items. In this way, time-sensitive, concurrent, new development operates to output the new product quickly. A project manager attempting a rapid introduction without the use of a well-structured database takes on unnecessary risk and is likely to incur unwanted delay.

Ron Kmetovicz's The One-Minute Time to Market Self Assessment, which identifies five key behavioral patterns exhibited by fast-moving new product development organizations, is available free to the readers of Electronic Design by contacting Time to Market at the address above.

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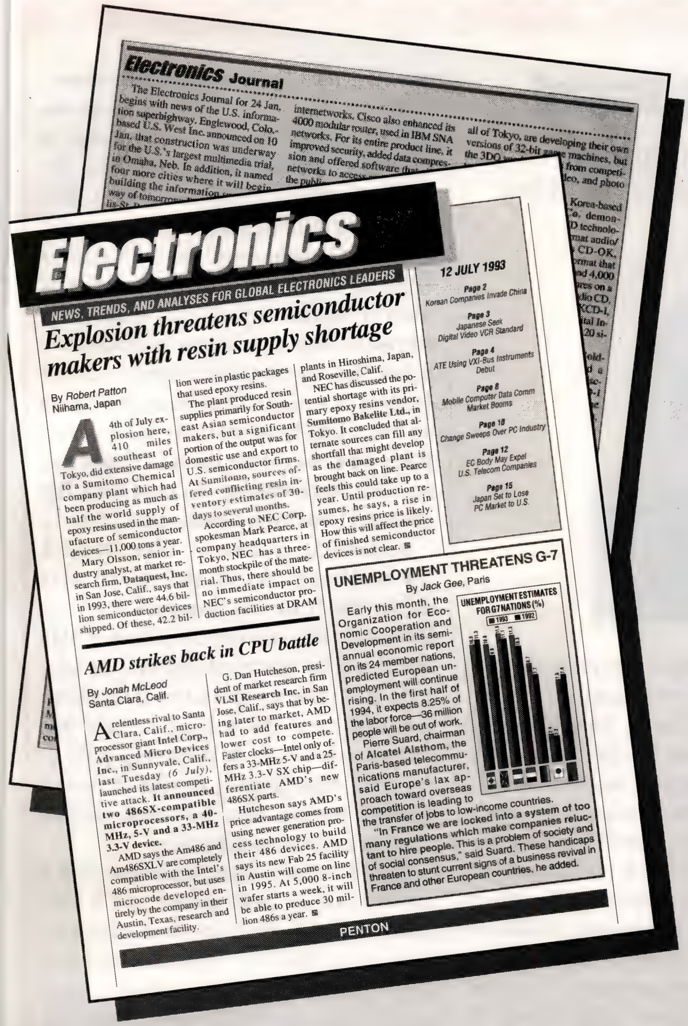

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin

internetworks. Cisco also enhanced its 4000 modular router, used in IBM SNA networks. For its entire product line, it improved security, added data compression and offered software

all of Tokyo, are developing their own versions of 32-bit

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

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Japan Set to Lose PC Market to U.S.

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms.

At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ▪

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ▪

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of **Alcatel Alsthom**, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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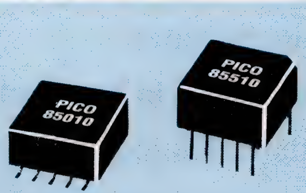

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MY VIEW

...Walking scared

BY FRANK J. BURGE
Director of Market Development for Electronic Design

Five weeks ago my roommate and I spent the weekend in Palm Desert getting in some R&R and golf. It was the 40th anniversary of our first meeting at a neighborhood saloon called the Cameo Lounge on Chicago's southwest side. It was a wonderful weekend even if she did beat me at golf. On our return to the Ontario Airport, I dropped off the luggage and my roomie went to check us in while I drove to the car return area.

After settling the paperwork, I started walking to the airport lobby. About 50 yards from the main entrance I came across a young man and his girlfriend, both probably in their late teens and is my custom I greeted both of them with a smile and a hello. With that the young man's face flew into a rage, and he asked me if there was something wrong. It scared the bejabers out of me, but rather than stop to chat with this lad with a giant chip on his shoulder, I ignored his remarks and kept walking; he began to follow me. My heart was pounding by the time I reached the main entrance, which was crowded with people. He stopped, stared angrily at me, and walked away. I had the feeling the guy wanted to stick a knife in my belly—for what I will never know. Maybe my imagination was running wild but I was plenty scared.

The funny thing is that I was born and raised in a big city and have always considered myself street smart. Whenever I visited New York or another big city, I always felt comfortable walking, even by myself, regardless of the time of day or night. I always had a spot picked out, an open business or a hotel lobby or someplace where I figured I could land if trouble found me. And I was careful to be aware always of what was happening around me. In all the years of walking in big cities—and what fun it is to walk in a big city—I never felt afraid. Only once when we were visiting Florence did I feel slightly intimidated when it became obvious that a bad dude wanted to make a run on my roommate and myself. But we managed to hustle into the doorway of a busy Italian restaurant where we had a bite to eat and then called a cab. When we came out for the cab the bad guy was still there waiting. He must have figured that I was even dumber than I looked.

America has become a violent place: A few months ago two college students were shot to death by two teenagers intent on hijacking their car. Months before, a high school student was murdered waiting for a train. And these are just a few of the senseless killings of law-abiding citizens who just happened to be in the wrong place at the wrong time. Random killings of visitors from Europe and Asia have made tourists think twice about coming here.

Consider that a young American does a graffiti number in Singapore and is sentenced to caning. Cruel and unusual punishment, some say, but when the pollsters asked Americans for their opinion, many voted thumbs up. Do it! In California, the politicians get instant applause with their "three strikes and you're out" legislation even though the grandstand play will bankrupt the state. And the death penalty, stiffer gun control, and crime packages du jour will likely be the basis of the next round of successful political campaigns.

My barber figures that some office seeker will even call for U. N. action on the theory that stemming violence in our cities is at least as important as doing so in Bosnia or wherever we are helping keep the peace this week. Here I am on the shady side of middle age and for the first time in my life, I was walking scared. That's no way to live. Yet walking scared is how millions of Americans live each day. Nutso.

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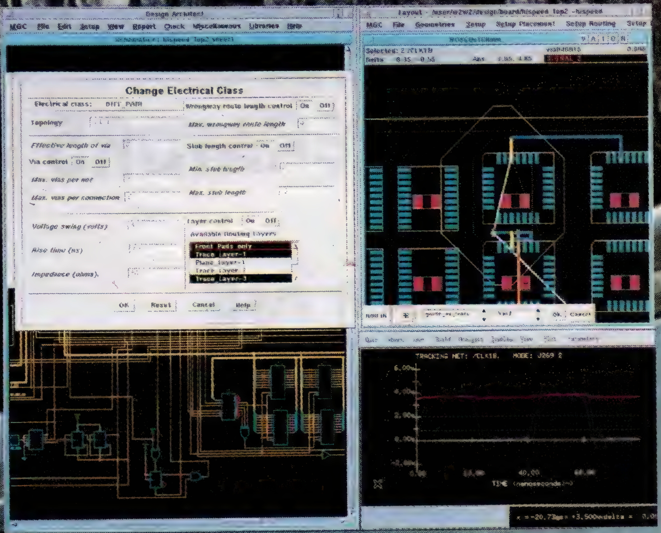
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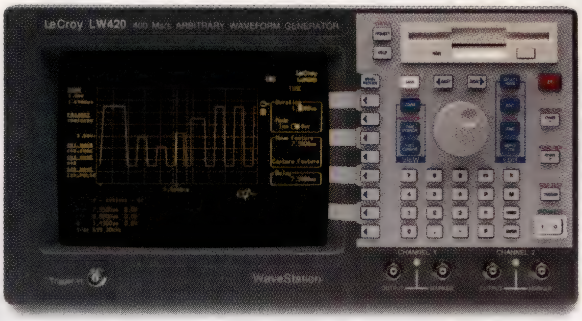

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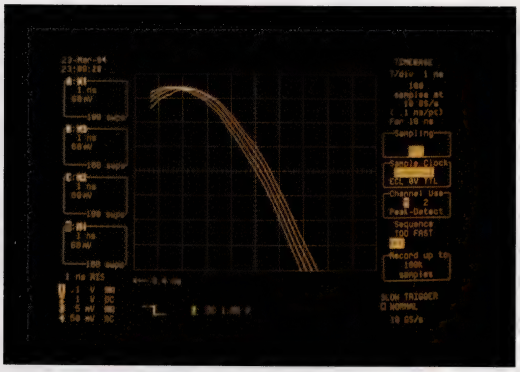

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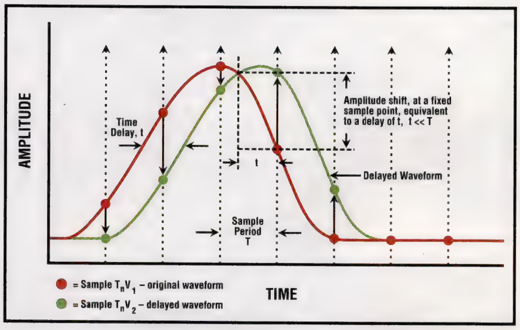
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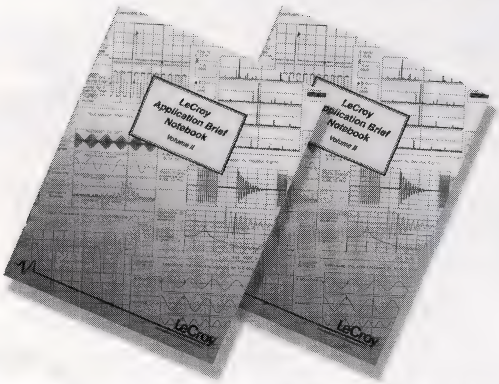
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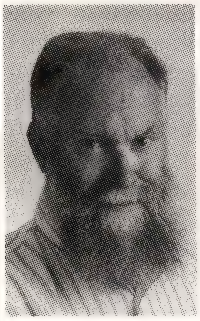
WHAT'S ALL THIS TELEDELTOS STUFF, ANYHOW?

I mentioned, some time ago, that Bob Widlar used to use his "Mexican computer," namely, Teledeltos paper. This is a kind of resistive paper that you could use to make analogs or analogues of various physical items.

Well, several people wrote in to ask, where can one buy some Teledeltos paper, these days? I checked around and found quickly that the last 3 places we had bought this paper were not in business any more. That's one of the problems you get when you buy a 5-year supply of something—after 4 years, you find that the guy has gone out of business—and, since you haven't bought anything for 4 years, no wonder.

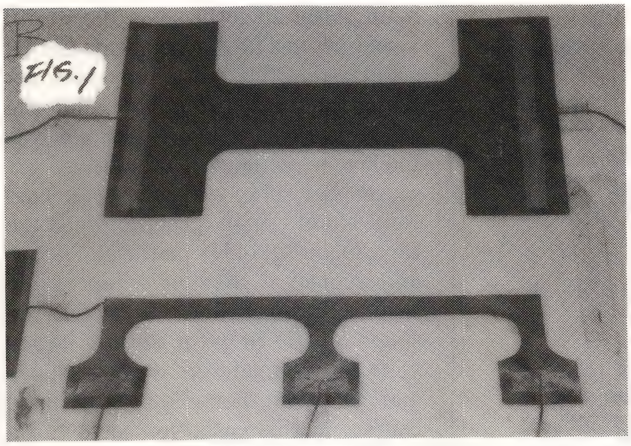


BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Our Librarian Mary Holland was agreeable to trying to help me find, where *can* you buy it? We still had several yards left, but we did not have enough to give or sell to all the people who wanted some. Mary did a search of businesses who might be selling anything by that trade name. No luck.

Then she started doing searches of the technical literature and journals. She found some Englishmen who had used it as recently as 6 or 8 years ago, in various technical studies.

Unfortunately, I was not able to contact any of those people to talk to.



But Mary did not give up easily. She searched for companies in the United Kingdom who might be making or selling this Teledeltos paper, and she found a company—Sensitised Coatings, Bergen Way, North Lynn Industrial Estate, Kings Lynn, Norfolk, England PE30 2JL.

After a little planning and negotiating, we were able to arrange a business deal, to keep it in a simple form, so anybody who wants to buy some Teledeltos paper can do it easily:

Simply buy an International Money Order for 44.00 pounds sterling (about $70). This pays for everything, including the paper, tax, packing, plus shipping, air freight to anywhere in the U.S.A.. (Unfortunately, the fee for the Money Order will be about $30, but that is an acceptable expense, if you are warned.) Send this money order to Mr. David Eatwell at the address above. This will soon get you a roll 29-in. wide by 45-ft. long, about 6 kilohms per square, Grade SC20.

Or if you send a money order for 36.50 pounds sterling, you can get a roll 18 in. x 59 ft., tax and air shipping included. Either way, the price per square foot is about the same, about 85 cents per square foot, fairly reasonable, as most experiments take only 1/2 or 1 or 2 square feet.

Now, while you are waiting for the paper to arrive, you have to get some conductive paint. You can buy 1/2 ounce of silver-loaded paint for about $36 from various hobby stores. The only problem with this stuff is, after you open it once, you come back in a month and it's all dried up. There are various kinds of conductive sprays or paints, and I do not have much luck finding them in stock, or getting them to work. At present, Planned Products, 303 Potrero St. (Suite 53), Santa Cruz, CA 95060 sells a new product, 1/2 ounce of silver-loaded epoxy (mix equal amounts of 2 components and it will cure in 10 minutes). I bought some, and it works well (about $14.95). You can phone them at (408) 459-8088. Also buy several inexpensive brushes and get some soft stranded copper wire.

OKAY—now that you have all this STUFF, what can you do with it? You can make a resistive analogue (or analog), a model of the physical thing you want to analyze. I have used it perhaps a dozen times since I was a sophomore at MIT, and on each of these occasions, it was exactly the right thing to do the job.

One of the early uses of this paper was to model the potentials in a vacuum tube. You paint onto the paper, a conductive pattern that represents the cathode, grids, and plate, and use conductive cement (or paint) to connect wires to those regions. Then you apply some voltages to the elements, and look for the patterns of the fields and the equivalent electron flow.

Now, you don't have to apply 300 V just because you are modeling a tube. This is an analog, remember, and if 5 or 10 V is convenient, then all the signals are proportional. You can

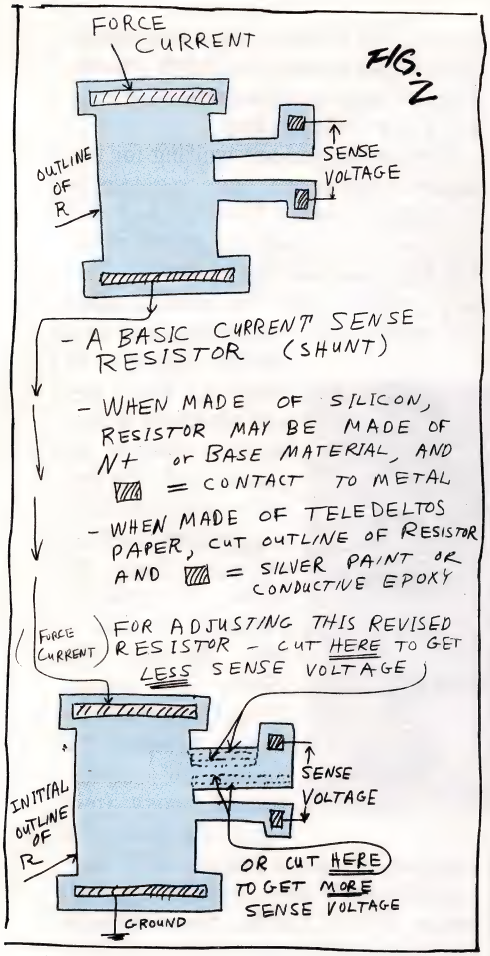


FIG. 2
FORCE CURRENT
OUTLINE OF R
SENSE VOLTAGE
- A BASIC CURRENT SENSE RESISTOR (SHUNT)
- WHEN MADE OF SILICON, RESISTOR MAY BE MADE OF N+ or BASE MATERIAL, AND ▨ = CONTACT TO METAL
- WHEN MADE OF TELEDELTOS PAPER, CUT OUTLINE OF RESISTOR AND ▨ = SILVER PAINT OR CONDUCTIVE EPOXY
FORCE CURRENT
FOR ADJUSTING THIS REVISED RESISTOR - CUT HERE TO GET LESS SENSE VOLTAGE
SENSE VOLTAGE
INITIAL OUTLINE OF R
OR CUT HERE TO GET MORE SENSE VOLTAGE
GROUND

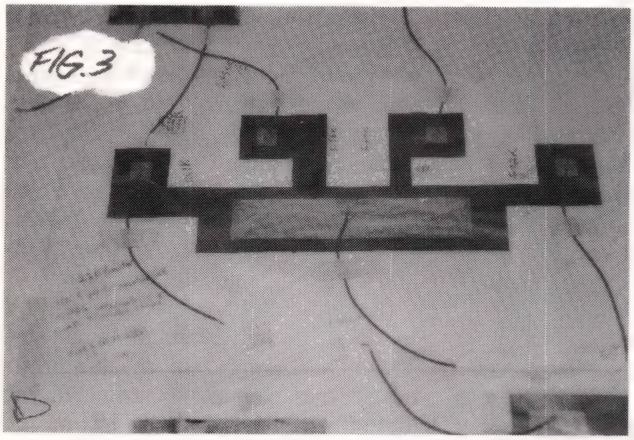
probe carefully to see where the equipotential lines are, using a sharp probe, very delicately. You can also conclude from this that the current flow is orthogonal to the lines of equal potential.

Figure 1 shows a typical example of how you can make an oddly-shaped resistor, where the outlines of the Teledeltos paper are cut, and contacts to the resistor are made with conductive paint. I've used it to compute the resistance of a low-ohms thin-film resistor with the smallest legal shape I could make. I painted along the ends of the unknown resistance. I just used a minimum amount of conductive paint to make the outline of the ends of the resistor. Then I made the outline of a simple rectangle so we could establish the sheet resistivity of the paper right adjacent to the experiment. After all, if the sheet resistivity varies 5% in a few inches, you can't be surprised.... Then we did some ratiometric tests and found what the resistance was. If the resistance was too low, we could slice off a little.

Another time, we made some current shunts with precision voltage taps, made out of N+ material. We had one geometry that gave repeatable results, and we wanted to change the shape a little to get a slightly larger voltage. We made up various shapes and compared them. See Figure 2. Of course, in this case, you have to be very careful not to nick the paper when you cut it, or you'll have a bad flaw in your analysis.

Figure 3 shows how Bob Widlar used this Teledeltos paper to define the sizes of several strangely-shaped emitter ballast resistors in his high-performance circuits. If there are any old-timers who have had other uses for Teledeltos paper, we will be interested to hear what they say.

I talked to Mr. Ken Eatwell, who worked with Teledeltos paper in its early days. He explained this paper was first developed in the United States by Western Union about 1936, as a paper sensitive to electric pulses, for the new Facsimile (Fax) machines. After the war, the Creed Co. (a subsidiary of ITT) started to make the "L39" paper, under license in England. Originally, the carbon-loaded paper was coated with dark gray lead thiosulfide, but for a better image, this was changed to a lighter gray copper thiocyanate. In the 1950's, Creed decided that the Fax business would never go anywhere, and got out of the business. Mr. Eatwell thought they were wrong, and started his company, Sensitised Coatings. These days, Fax machines use thermally-sensitive paper, or plain paper with a laser engine or ink jets.



Now is this paper adaptable to a 3-dimensional study? Generally not. I would love to have some 3-dimensional resistive stuff, to help me estimate thermal impedances and thermal cross-talk on an IC die. But I don't think the Teledeltos paper gives me any help there.

Three-dimensional flow is a whole 'nother ballgame. I have thought about making a capacitive analog using a large tub of oil in the shape of a die, with little electrodes in the shape of the heat sources. I am sure I could do this, but I haven't gotten exactly desperate enough to make this one. Besides, one spill and I'd be banned from our lab for life.

Could a powerful modern computer do any or all of this work? Quite possibly, using Finite Element Analysis. But if there is an error in there, you are not likely to find it. If you make an error with Teledeltos paper, you have to think about the shape of the curves, and you may get enough insights that you would catch a mistake. Also, for certain kinds of geometries, the Teledeltos paper may be really easy to apply, when defining the shapes for a computer might be excessively hard.

Is the Teledeltos paper really the hard way, the old-fashioned way? Maybe it seems old-fashioned, but if it gives you some good insights, then it may be a superior technique. And it may be easier than typing a whole bunch of data into a computer.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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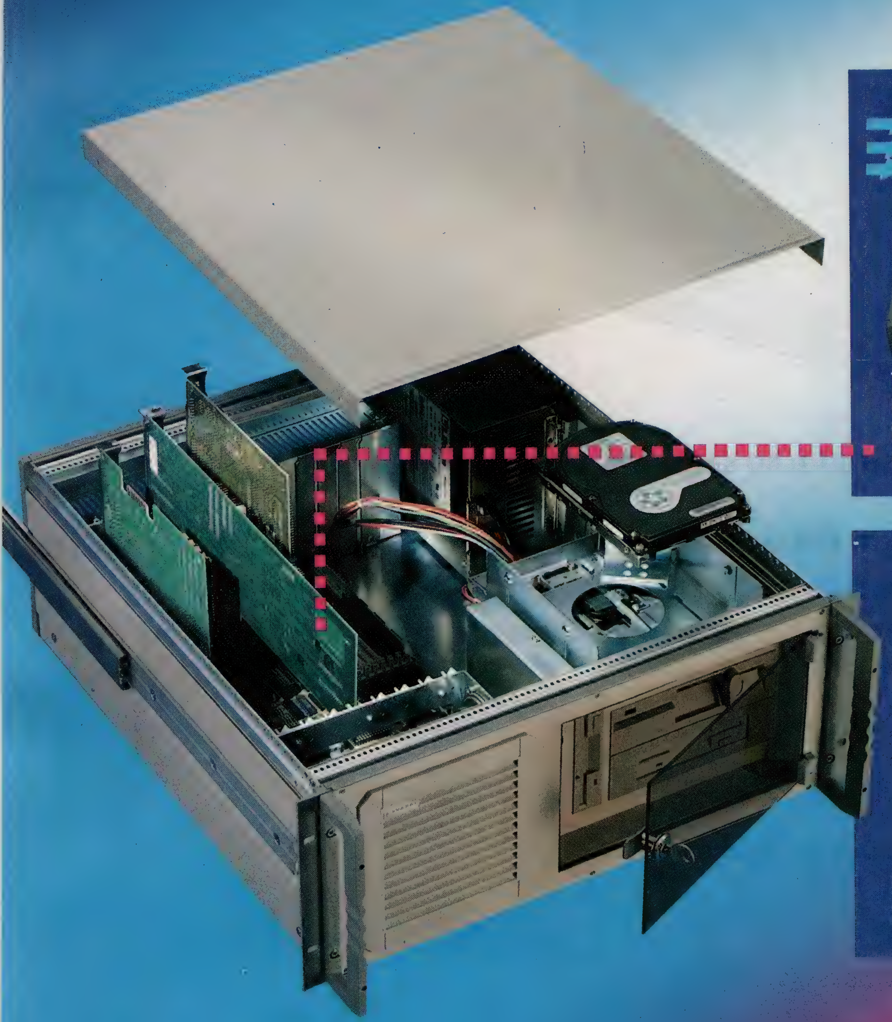

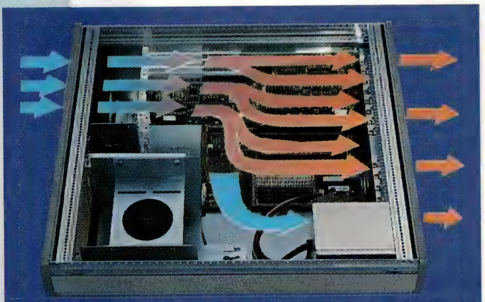

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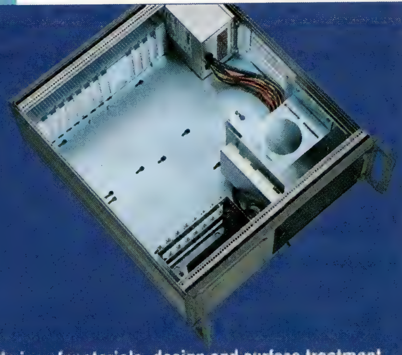

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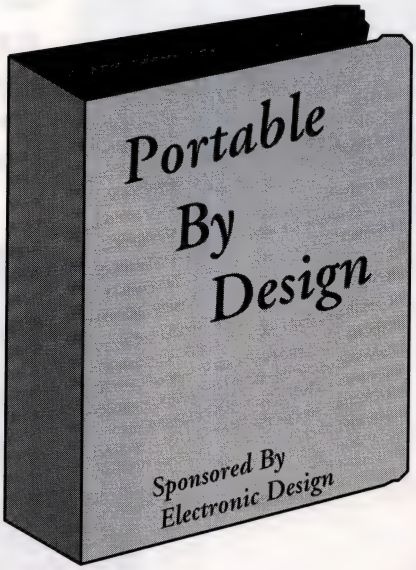

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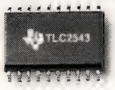
TI's new TLC2543 12-bit A/D converter at a 10-bit price.



The TLC2543 from Texas Instruments sets a new price/performance point in the marketplace. Its power dissipation is only 5 mW typical. That's 50 percent ower than most 12-bit A/D converters, at about half the cost.

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TLC1549	5.0 V	1 ch/serial	21 µs	10 bits
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TLC1541/43	5.0 V	11 ch/serial	21 µs	10 bits
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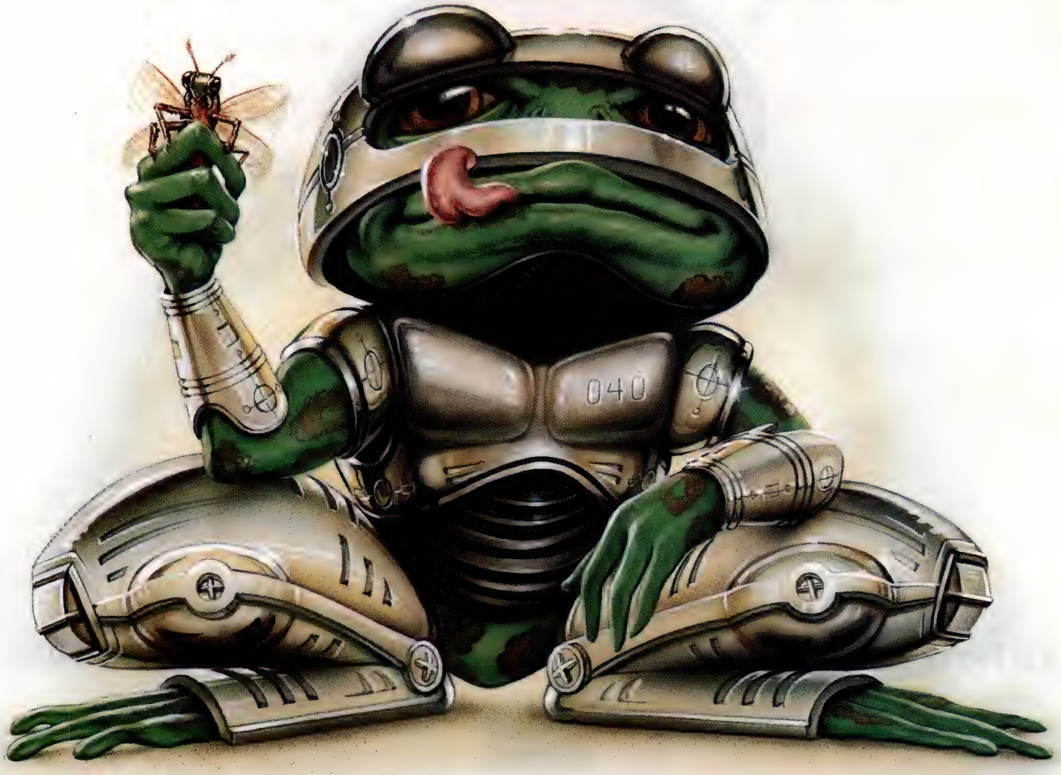

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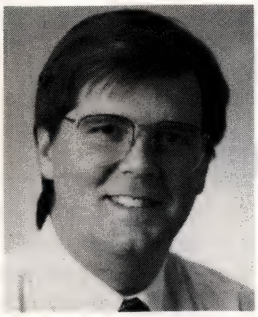
PC GRAPHICS WATCH

PnP ON THE VL-BUS

DAN HAAB, DAS INC.

The Plug and Play (PnP) specification developed by Microsoft and Intel lets end-users upgrade their PCs without having to configure any hardware or worry about any conflicts. Users simply plug in the peripherals, such as graphics cards, LAN adapters, and hard-disk controllers, and the machine configures itself. Windows 4.0, which may appear by the end of this year, will incorporate the necessary software to implement Plug and Play. The VL-Bus has responded by releasing the VL-Bus Plug-and-Play Addendum. The addendum, which required some assistance from Microsoft, gives peripheral manufacturers the information needed to design and implement VL-Bus PnP-compatible peripherals.



By extending the ISA PnP 24-bit address space to a 32 bits, existing ISA Plug and Play and VL-Bus specifications are fully compatible. This makes the VL-Bus PnP addendum a transparent addition to Microsoft's PnP ISA specification, maintaining the VL-Bus goal of software transparency. Therefore, VL-Bus PnP peripherals can be inserted into an ISA PnP-compatible system and work with the existing ISA PnP software.

The VL-Bus PnP concept is built around four states: Wait for Key, Sleep, Isolation, and Config. When the system is first powered up, all cards start in the Wait for Key state. At this stage, the cards' outputs are disabled while they wait for an initiation key. The Sleep state begins after the initiation key is received. The card remains in the Sleep state until it's isolated during the isolation procedure. After a card is isolated, it receives a unique Card Select Number (CSN) and its resources are read. After all cards in the system are isolated, they're set to the Config state and system configuration takes place.

For these states to occur, three special PnP registers have been defined: Address, Write_Data, and Read_Data. The Address register is "write-only" and monitors the initiation key. The Write_Data register, which also is write-only, writes configuration data to the card. The read-only Read_Data register obtains the cards' resources and unique serial identifier.

At power up or system reset, all PnP cards set their CSN to 0, disable all outputs, and wait for the initiation key. The system will boot using the power-on defaults for the PnP boot device. The remaining PnP cards won't respond to any accesses until the initiation key is received. The initiation key is a 32-byte series of I/O writes to the Address port. The card must monitor all I/O writes to this port and check for a match with the initiation key. The initiation key, which is specified in the PnP ISA specification, is the same for VL-Bus PnP. The VL-Bus PnP cards must monitor I/O write cycles to the Address port and wait for the initiation key, but they can't drive the $\overline{\text{LDEV}}$ or $\overline{\text{LDRY}}$ signals. Driving the $\overline{\text{LDEV}}$ would cause the I/O Write output to be captured locally, preventing it from reaching the ISA bus.

Once the initiation key is received, the card must participate in an isolation procedure, which is enabled by a 72-bit serial identifier that's unique to each card. The identifier consists of two 32-bit fields and an 8-bit checksum. The first 32-bit field is a vendor's identifier, while the second field contains a card-specific serial number or other card-specific data. The isolation sequence begins with an I/O read to the Read_Data port. The serial identifier is located in a shift register, with the first bit at the shift register's output.

If the shift register's output, referred to as the current bit, is a 0, the card puts its outputs in a high-impedance state. Cards with a 1 as the current bit will drive the bus with data signifying 55h. Another read to the Read_Data port is then executed. Again, cards with a 1 as the current bit drive the bus, but this time with an AAh. All cards in the high-impedance state monitor the first two bits in the data bus to see if another card responded to the previous reads. If those cards detect such a response, they remain in the high-impedance state waiting for the next iteration of the isolation procedure. The serial identifier is shifted 1 bit and the sequence is repeated. After 72 pairs of I/O reads occur, only one card will remain. This card is assigned a CSN and put in sleep mode. The procedure continues until all PnP cards are identified.

The isolation procedure becomes slightly different when accommodating VL-Bus PnP cards. Because the ISA and VL-Bus cards reside on different buses, the isolation procedure must be done separately for each bus. The procedure begins as outlined above, but if a VL-Bus PnP card is present, it will drive $\overline{\text{LDEV}}$ and $\overline{\text{LDRY}}$ for the read cycle. The driving of these signals isn't seen by the ISA cards because the cycles captured by a local device asserting $\overline{\text{LDEV}}$ never reach the ISA bus.

Designing To The Plug and Play SCSI Standard

PnP design profile complements maturing SCSI standards.

BY JEFF EPSTEIN and
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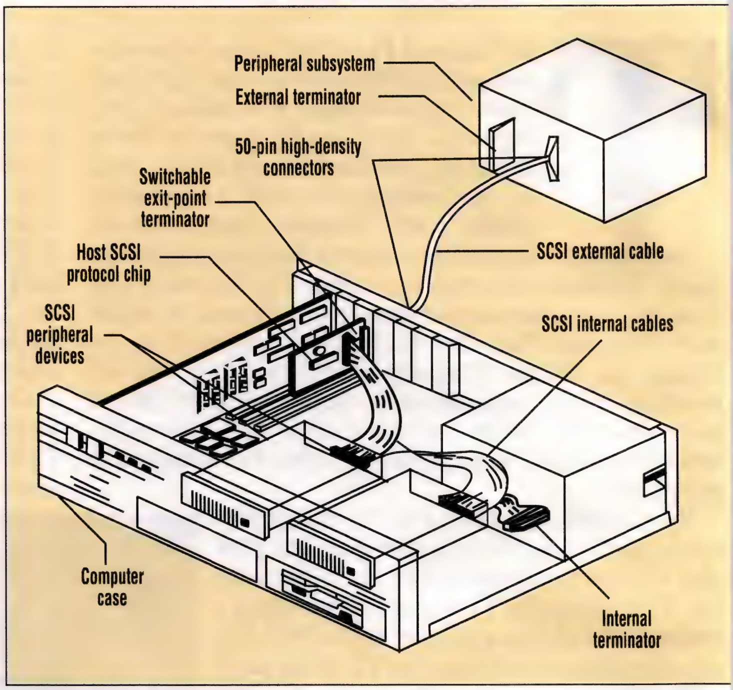
STEVE TIMM
Microsoft Corp., One Microsoft Way, Redmond, WA 98072.



1. Self-termination in a PnP system is achieved using a standard cable configuration. An active termination component resides at the internal cable end, and a second exit-point terminator is located on the host adapter.

The SCSI interface is known for it's breadth of device support, range of performance options, and external peripheral expansion. Yet it's difficult for many PC users to configure add-on SCSI devices because the process typically requires setting board-level jumpers, switches, and setup utilities in the configuration sequence. Consequently, SCSI has become a target for Plug and Play (PnP) designs, enabling users to quickly and easily change peripheral configurations to meet their personal computing needs. For SCSI product vendors, PnP pledges consistent design parameters, enhanced device interoperability, and lower support costs.

Within the PC architecture, supporting PnP developments will enable jumperless design of add-in SCSI cards, including PnP ISA, PCI, etc. Such support encompasses a PnP BIOS and PnP OS to fully automate the configuration of SCSI devices. For example, system resources like interrupt requests (IRQs), address spaces, and DMA channels are automatically assigned to boot devices by the PnP BIOS. Non-boot PnP SCSI devices and software drivers are automatically configured by the PnP OS during initialization.

Following the path set forth by the PnP BIOS and ISA capabilities, industry leaders such as Adaptec, Future Domain, Maxtor, Microsoft, and NCR proposed PnP SCSI. After some refinement, Rev. 1.0 of the specification, which is targeted for volume PC applications, was released this past March. While the SCSI-3 standard specifies component-level requirements, PnP SCSI defines system-level design parameters that are essential for automatic configuration of SCSI devices. PnP SCSI also outlines designs for PC SCSI subsystems, host adapters, and peripherals, including disk, tape, and CD-ROM drives. Primary components of a PnP SCSI system are a cable connector, SCSI-bus automatic electrical termination, and SCSI-ID automatic configuration during the platform's boot process.

Electrically, the SCSI bus exhibits the noise characteristics of a transmission line. Assuming an electrically consistent set of cables, connectors, and printed-circuit stub lengths per SCSI-3 parallel interface (SPI), a chain of SCSI devices can effectively terminate the bus by activating termination components located at each end of the bus. PnP offers a digital solution for an analog problem that requires dynamic adjustment whenever the SCSI configuration changes.

A PnP SCSI chain internal to the PC enclosure must be self-terminating. This allows external expansion without having to remove the system cover. Self-termination is achieved using a standard PnP cable configuration with an active termination component at the internal-cable end, and a second exit-point terminator located on the host adapter *(Fig. 1)*. PnP eliminates the cost and complexity of having each peripheral supply bus termination. Instead, individual termination components are replaced by a system designed for

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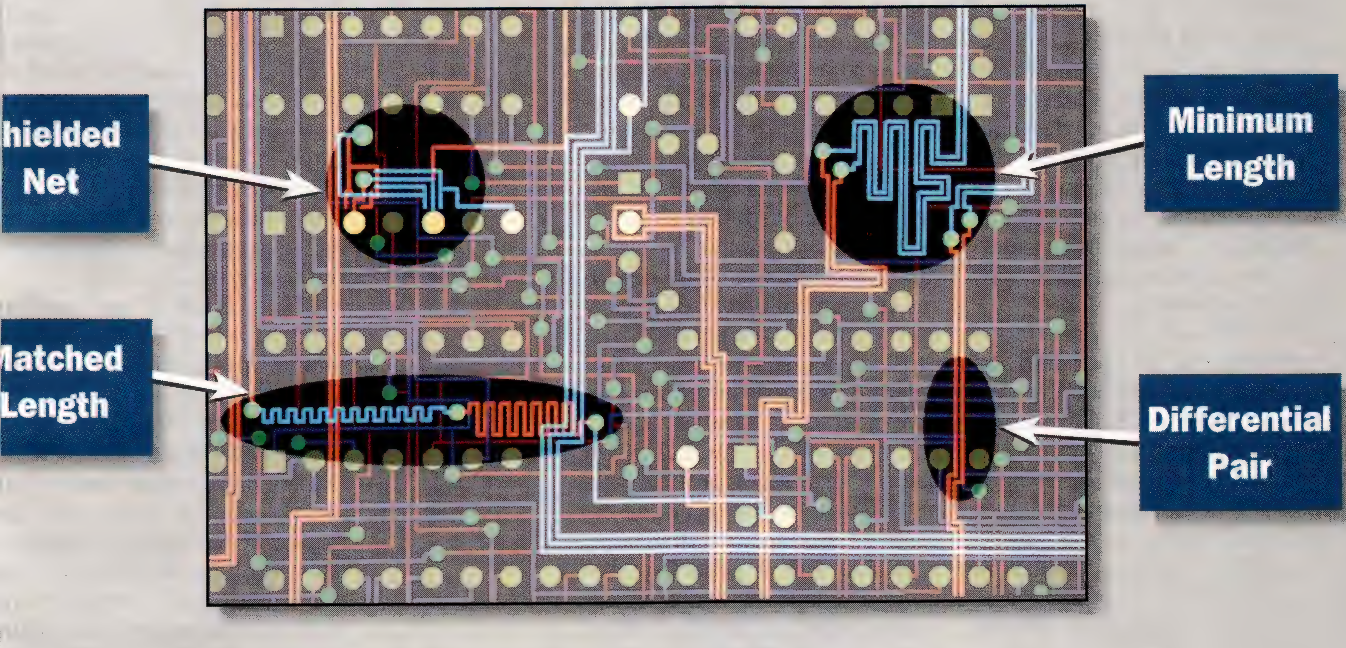

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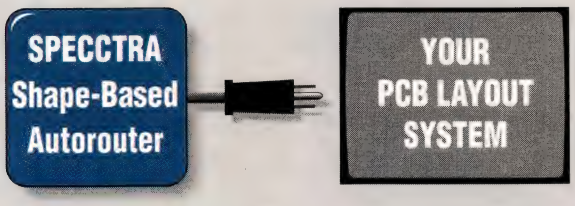

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bus termination.

Internal SCSI buses that are routed to an external SCSI connector require some form of automatic termination. The exit-point terminator, located conceptually at the mid-point joining the internal and external SCSI buses, must be enabled whenever an internal- or external-only SCSI chain is attached to the host adapter. For a mixed SCSI configuration, the exit-point terminator must be disabled when a peripheral device is attached to the external SCSI connector. This allows the internal bus to be extended outside the PC enclosure.

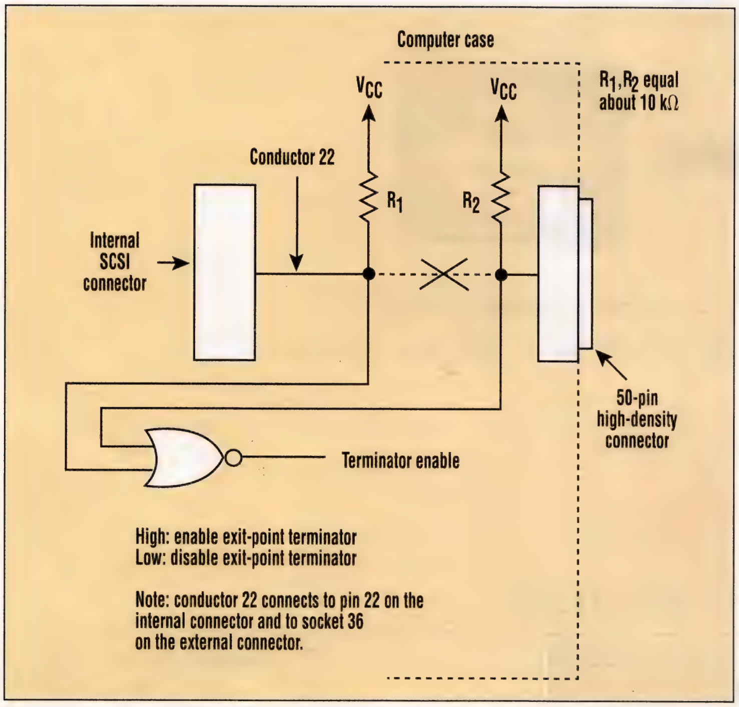
In this scenario, an external terminator is plugged into the only open connector on the external chain of SCSI devices. The automatic termination component should be located close to the exit-point connector to avoid excessive stub lengths from affecting signal quality. In some cases, this terminator may need to be integrated into the exit-point connector assembly.

One approach to PnP termination senses the current flow on the reset line to determine if the lines are terminated properly. The termination circuit connects directly to both connectors and a third contact is separated from each connector by a 5-Ω resistor for current sensing. During the reset cycle, the termination circuit senses the current sink to each connector. If the current from either connector is less than 10 mA after 1 μs, the termination component is activated, pulling the line high. Termination components supporting this technique are currently being developed. One such part comes from Dallas Semiconductor (#DS2109).

Another approach to automatic termination is to detect the attachment of a SCSI device on the external connector. If no SCSI device is attached to the external PC enclosure, then the host adapter is located at one end point of the internal SCSI chain. This requires that the automatic termination circuit be enabled. Connectors that support this technique activate a ground signal when an external cable is attached. Though effective, this mechanical solution suffers the fate of introducing yet another connector with low-volume pricing.

An alternative design for PnP termination is a low-cost circuit that consists of a pull-up resist attached to a single ground li on each of the adapter's SC connectors *(Fig. 2)*. Pin 22 used on the internal connecto while pin 34 is employed on t external. These two signals driv the control logic on the ho adapter's termination circui The switchable active termin tion component is disable whenever both input signals a low, indicating a device on th internal and external SCS chains. If either input signal i high, then the terminator is en abled to terminate one end of th internal or external bus.

This circuit is an excellen choice for PnP SCSI host adapt ers and also is effective for multi initiator systems as long as th adapters are separated by a least one SCSI peripheral. Whil satisfying requirements for Pn SCSI adapters, additional de sign will be required to exten this termination concept to a SCSI peripherals because it re lies on adjacent devices to main tain the SCSI ground signals Another possible constraint i bus loading. And for fast SCS timing, multiple disabled auto matic-termination component could affect timing margins.


Computer case
V_{CC}
V_{CC}
R_1,R_2 equal about 10 kΩ
Conductor 22
R_1
R_2
Internal SCSI connector
50-pin high-density connector
Terminator enable
High: enable exit-point terminator
Low: disable exit-point terminator
Note: conductor 22 connects to pin 22 on the internal connector and to socket 36 on the external connector.

2. An alternative PnP termination circuit consists of a pull-up resistor attached to a ground line on each of the adapter's SCSI connectors. A simple modification is required because the connector will be attached to an external peripheral.

All SCSI devices require unique SCSI ID that' currently set by a switch on older "legacy" devices. Conflict occur when two or more device have the same ID, resulting i the controller's failure to recognize one or both devices. Thi condition forces end users to review switch settings for the entire SCSI chain or to randoml change ID switches until th system works. To solve thi problem, the ANSI SCSI committee defined a protocol calle SCAM (SCSI Configured Automatically) that allows PnP peripherals to have their SCSI ID automatically assigned by a Pn host adapter.

During the isolation stage, th SCAM Master isolates each SCAM Device one at a time and stores the device's Default ID

IF IT SHAKES RATTLES OR ROLLS OR SPINS RECORDS PUSHES PULLS COMPRESSES TRANSFERS MEASURES PLACES SHIFTS PRINTS DROPS GRINDS SWAPS PLAYS LIFTS SPLITS BAKES CUTS ETC. ETC. ETC.

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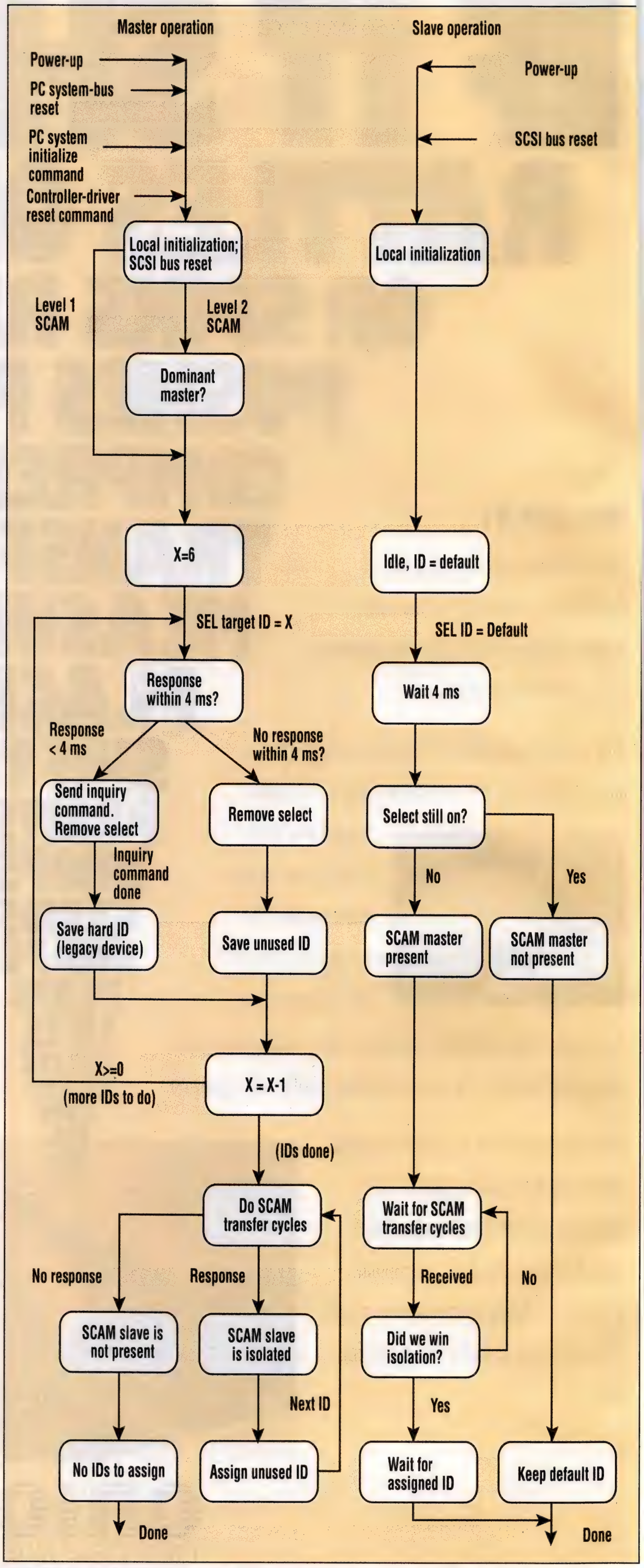
The 5-bit ID field within the Type Code contains the device's Default ID. The SCAM Master assigns the SCAM device a Soft ID after its isolation stage is completed and before isolating the next SCAM device.

The SCAM Master assigns Soft IDs that are not already used by another bus device. The first choice is the device's Default ID. If that's taken, the next smallest number is used. If zero isn't available, wrapping around to a choice of six or smaller should be assigned. If no choice is possible, the device's Soft ID remains unassigned.

Devices supporting the SCAM protocol are 100% backward-compatible with the installed base of legacy SCSI peripherals. Legacy devices retain their default IDs based on jumper settings because these IDs aren't programmable. In the reverse scenario, PnP SCAM peripherals connected to a legacy host adapter respond to their Default (jumpered) ID just like today's legacy devices. While SCAM defines two levels of functionality, PnP SCSI requires Level 1 only. Level 2 incorporates provisions for multi-initiator support and response to ID assignment requests from late-arriving (hot-plugged) SCSI peripherals.

Generally, only firmware changes are necessary to implement the SCAM protocol. However, there are a number of hardware design considerations. First, the SCSI-interface silicon must be able to drive the state and timing of data and control signals under program control. While many chips do this, some will require a redesign to support SCAM. Second, PnP will likely require an additional 2 kbytes of ROM space to implement the protocol. Third, SCSI ID switches will need to remain accessible on the peripheral device to allow for backward-compatibility with the installed base.

The necessary timing characteristics generally aren't difficult for designers to incorporate



3. The flow charts show the master and slave operation of the SCAM protocol and all of the states that must be considered. The information holds true whether the peripherals are internal or external to the platform.

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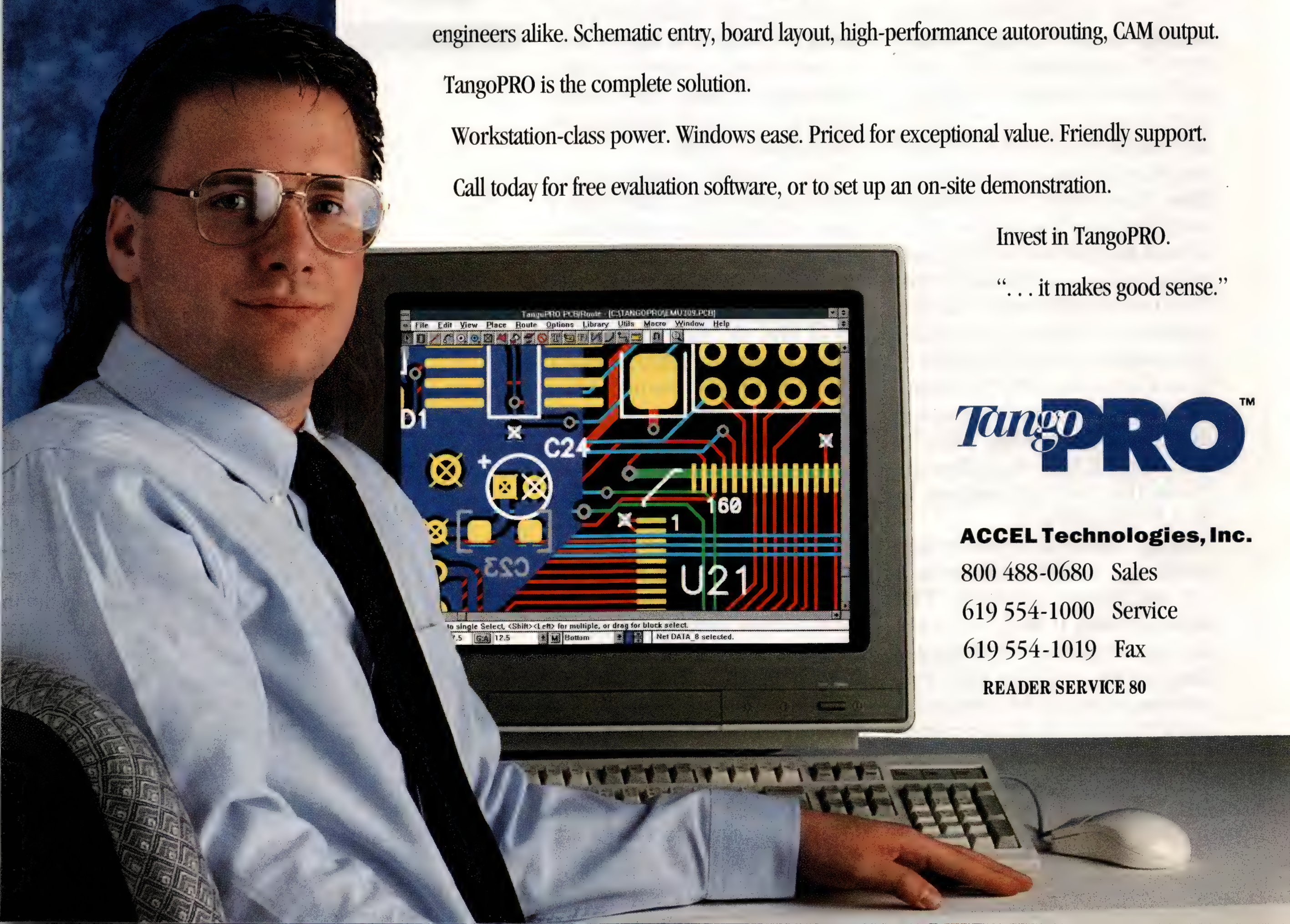

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within the firmware of the host controller or peripheral device. One characteristic that's somewhat interesting is the delay responses to Default ID. A peripheral usually responds to its ID selection as soon as possible. For SCAM, the PnP peripheral must wait at least 4 ms before responding. This delay is used by the host adapter to distinguish PnP peripherals from legacy peripherals with non-programmable IDs.

SCAM requires several states to perform the bus protocol *(Fig. 3)*. However, because the SCAM protocol defines new BSY/SEL/MSG states on the bus, some debug-analysis test equipment will be unable to detect the new states. To aid the designer, capable SCAM Protocol Analyzers are available from Ancot Corp., Menlo Park, Calif. The host controller first determines if it's to be the "dominant master." This operation is optional for SCAM Level 1, which doesn't use multiple hosts.

The host adapter then queries or scans the bus looking for non-SCAM peripherals. The host performs a normal arbitration/select sequence for each ID value, ranging from 0 to 6. SCAM peripherals will automatically delay 4 ms before responding to their Default ID selection. Non-SCAM peripherals will respond immediately in less than 4 ms. This timing difference makes it possible for the host to differentiate between a mixed configuration of legacy and PnP peripherals. The host adapter must save the ID values already used by the non-SCAM peripherals. These IDs can't be assigned to SCAM peripherals.

Next, the host adapter performs the SCAM isolation and ID assignment protocol. The data-bus bits, 0 to 7, are used during isolation for multiple bus-transfer cycle handshakes, allowing data to be communicated between the host controller and the peripheral *(Fig. 4)*.

The handshake timing uses DB_{0-4} for data and DB_{5-7} for handshake control timing. For each field transfer, the most significant bit and byte are sent first. During the isolation process, a SCAM target uses its standard SCSI Inquiry Identifier string to differentiate itself from all other SCAM targets on the bus. It does this by performing each data-transfer cycle transmission in a bit-serial fashion using only two lines: DB_0 and DB_1. However, the host controller uses all five DB lines for its transfers.

The target-bit serial coding can be considered an arithmetic comparison that's done bit-serially. For the first serial transfer, each target checks the first bit of its own Inquiry string. If the first bit is a 1, the target drives the DB_1 line, otherwise it drives the DB_0 line. If one or more of the targets has a 1, then the process will proceed to the second bit. If all of the targets had a 0 value for the first bit, then the process will proceed to the second bit. If the DB_1 line is driven by one target, but other targets had a 0 Inquiry string bit, then that target may be considered to have a lower arithmetic string. The target drops out of the isolation process because it "lost."

The bit-serial compare process repeats until each target runs out of Inquiry string bits. When there's no more bits, it ceases to drive either the DB_0 or DB_1 line. When all targets run out of bits, the host knows that one of the targets had the largest arithmetic Inquiry string value. Hence, it isolated one target from the remaining targets.

The ID assignment process follows the isolation process. The host sends an ID to the winning target using the DB_{0-4} lines. The host then repeats the full isolation process for all remaining SCAM targets that don't have their IDs assigned. When all IDs are assigned, no duplicates or conflicts exist.

Another PnP design alternative stems from PnP SCSI's requirement for host adapters to consistently assign SCSI IDs t maintain a consistent boot-device and drive letters. This ca be done by using the SCAM I assignment algorithm called ou in the PnP SCSI specificatio (section 6.4.3) or, as an option by using nonvolatile RA (NVRAM) on the host adapter The NVRAM tracks the SCS IDs and drive number assignments (80h, 81h, etc.) for unique device ID string derive from SCSI inquiry data.

The SCAM protocol allows PNP peripherals to have their SCSI IDs automatically assigned by a PnP host adapter

While NVRAM isn't required for PnP SCSI, it can eliminate drive-letter changes tha result from the addition of a peripheral device to the SCS chain. NVRAM also can maintain the boot device once a second boot drive is incorporate into the system. In the shor term, system designers shoul select a motherboard PnP BIO manufacturer that allows ATA/ IDE disk drives to coexist with SCSI drives. Then users can select either one for boot purposes without disabling the other. In the longer term, PnP will require a platform-independent system architecture to select the boot device and channel, such as IDE, SCSI, or PCMCIA.

PnP SCSI peripherals eliminate the need for users to set switches or disassemble the unit when reconfiguring the system. Hardware requirements include designing in a self-resetting circuit for "term power," disabling internal termination components, and exposing two 50-position high-density connectors on the external peripheral enclosure. Polyfuse devices, such as the RBE130 developed by Raychem Corp., Menlo Park, Calif., work well for printed-circuit applications. Removing termination components from the internal device can reduce cost, but in the short term, peripherals must maintain their ID switches to be compatible with legacy devices.

A key requirement for PnP SCSI peripherals is the firmware implementation of the SCAM Slave protocol described earlier. The amount of additional code

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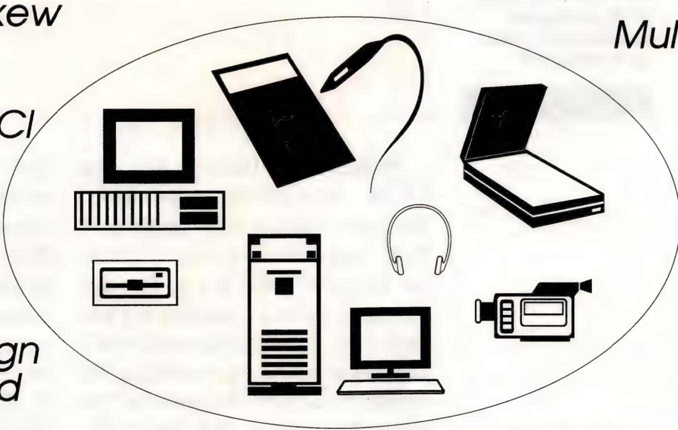

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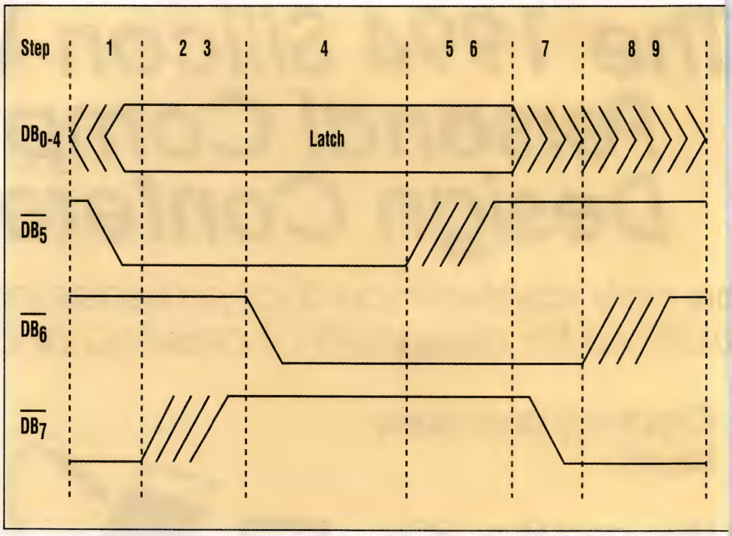
most likely won't raise the product's manufacturing cost. Also, existing peripherals that use flash memory for firmware allow for SCAM firmware upgrades. In the software arena, standard command sets for SCSI peripherals are spelled out in the formal ANSI SCSI-2 specification. For PnP, command sets are being refined so that given devices can interoperate with a common device driver. Current work is heavily focused on CD-ROM drives, but other devices are planned.

SCSI integrated onto the motherboard is the best choice for PnP because it eliminates the cost and configuration of an add-in host-adapter card. This configuration requires integrating the SCSI-controller manufacturer's BIOS code into the motherboard's BIOS code. For add-in cards, PnP system components, including a PnP BIOS and OS, fully automates SCSI adapter installation.

Cabling is another key issue for PnP SCSI systems. Today, five popular SCSI connectors result in up to 15 different cable configuration choices. The 50-position high-density connector was chosen for PnP for its small footprint, low cost, and high volumes, coupled with the acceptance of fast 8-bit SCSI. However, PnP SCSI may consider adopting the 68-pin high-density connector for future workstations if a standard icon can be displayed on the connector for future workstation applications. Note that PnP doesn't specify connectors internal to the PC or to the peripheral enclosures.

Another PnP design parameter is the automatic negotiation of transfer protocols. Host adapters must automatically accommodate the various SCSI Bus synchronization protocols, including asynchronous, synchronous, and fast synchronous. The PnP specification recommends that the host adapter negotiate with the peripheral for the protocol to be employed in the data transfers.



4. Data-bus bits 0-7 are used for multiple bus-transfer-cycle handshakes during isolation on the SCSI bus. This data is applied when the SCAM (SCSI Configured Automatically) protocol is employed.

When negotiating for the SYNC data-transfer operation, the host adapter first sends a 5-byte Synchronous Data Transfer Request (SDTR) to the peripheral. Byte 2 contains the actual sync request code and byte 3 holds a number representing the transfer period. The smaller the value for byte 4, the faster the transfer period. For fast SYNC operation, a typical value for byte 3 may be around 19h. For slower SYNC operation, it may be 35h. The adapter firmware maintains a table containing the appropriate values for the various devices it supports.

If the peripheral returns a Messenger Eject signal, then the peripheral is notifying the adapter that it doesn't support that particular speed of SYNC operation. Hence, the controller must keep sending SDTRs with larger numbers until the target accepts the message. If the target ultimately doesn't accept any of the various large numbers, the controller and target default to ASYNC operation. Most fast SYNC targets return a multiple byte message that spells out the preferred value for byte 3. In this scenario, the adapter and peripheral directly establish the fastest possible SYNC data-transfer operation.

The PnP specification supplies a compliance checklist for peripherals, host adapters, and systems. However, to realize the goal of PnP SCSI, additional work is in progress to define an standard compliance-test procedure. Such procedures could be used by device vendors with cross checks by adapter vendors to ensure interoperability between a matrix of legacy and PnP devices. Beyond individual device testing, certification of PnP devices for a PnP OS will broaden the test matrix and include PnP device drivers for optimum compatibility assurance.

For further information on PnP SCSI, Compuserve contains the PnP SCSI specifications, SCAM Revision 5, and a support forum. For access, type GO PLUGPLAY. In addition, there's a SCSI BBS located at 719-574-0424.

Steve Timm, storage technical evangelist for Microsoft's Personal Systems Group, holds a BSEE degree from Michigan State University, East Lansing.

Jeff Epstein, a senior project engineer at Future Domain, holds a BSEE from the University of New Mexico, Albuquerque, and an MS in computer science from the University of California at Los Angeles.

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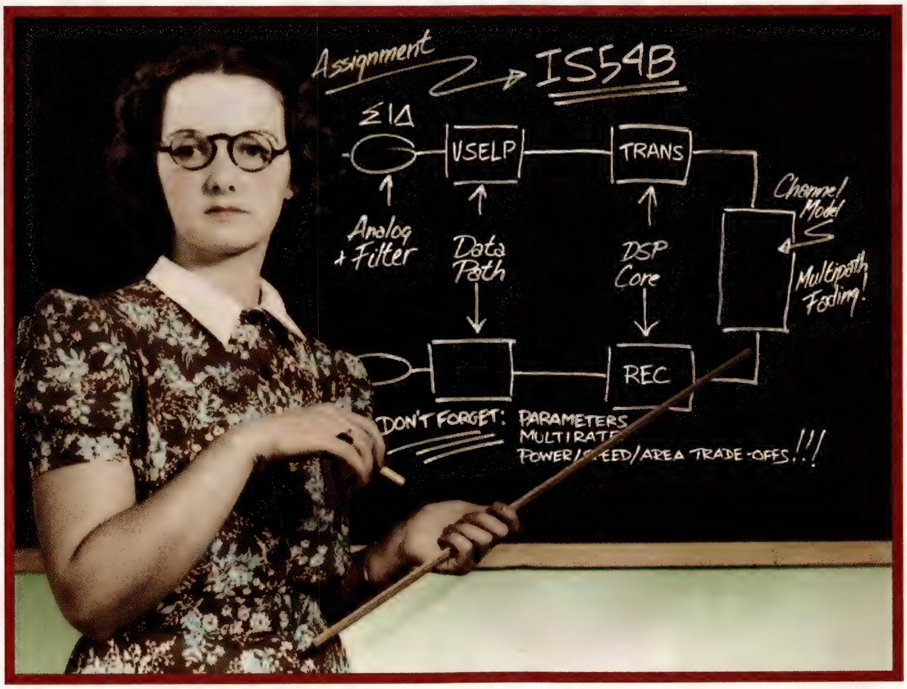

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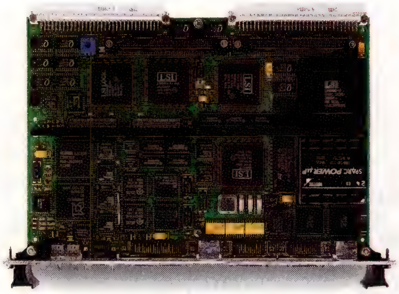

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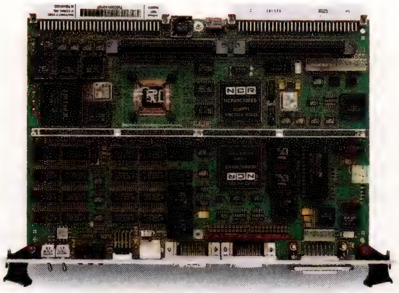
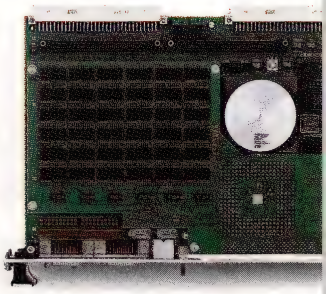


CPU-3CE
lowest cost SPARC CPU



CPU-10
high performance, rugged form f

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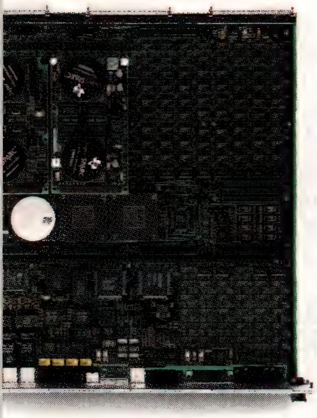
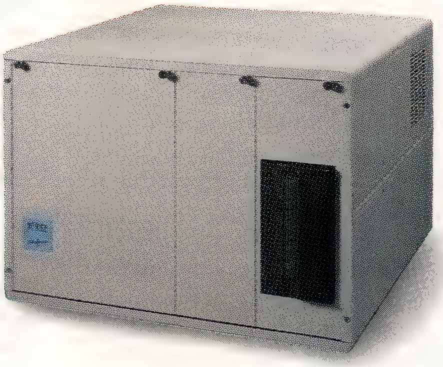
ARC 94



CPU-10/9U
mory intensive multi-processing



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industrial system

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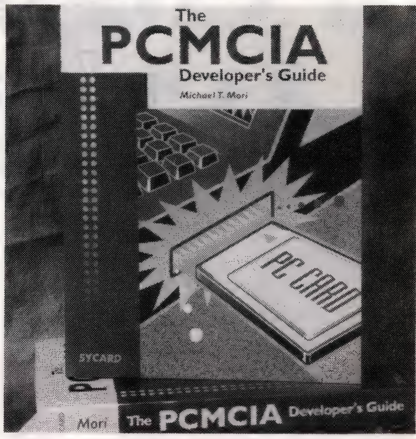
SYSTEM DESIGN NEWS

Small-format personal digital assistants and subnotebooks often achieve their small sizes by limiting expandability. Typically, they will include only one PCMCIA card slot for user-added options like modems. Now, Smart Modular Technologies, Fremont, Calif., has come up with a designed-to-order Type II PCMCIA card that holds both memory and a fax/data modem. This eliminates the need to repeatedly swap cards when moving files from the modem to host memory, and then to removable memory. The card holds 2 to 4 Mbytes of nonvolatile, electrically reprogrammable flash memory. About 40 fax pages (assuming 40 kbytes/page) plus other information can be stored with 2 Mbytes of flash. The modem contains high-level error correction and data compression, and performs 2400-bit/s full-duplex data communications and 9600-bit/s fax transfers. User-available features include auto-dial, auto-answer, and fallback for compatibility with slower modems. A DAA interface is included. The modem's flash memory holds the operating firmware and incorporates a battery-saving, low-power sleep mode that trims current drain to just 2 mA. In single-unit lots, the 2-Mbyte version of the combo card sells for $349; the 4-Mbyte version lists for $449. Contact Bill Johnston at (510) 623-1231.

Sparc-based processor boards for embedded applications—the same cards powering the recent SPARCstation System 5 and System 20—will double the throughput of previously available SPARCengine boards. Not only do the boards increase throughput, but the price for the lowest-cost SPARCengine card, the SPARCclassic engine, has dropped to $1900. The SPARCengine 5 motherboards are the first with the microSPARC II processor and operate at 70- or 85-MHz clock rates, delivering 57 and 64 SPECint92 and 47.3 and 54.6 SPECfp92, respectively. The boards include the new AFXbus interface for 64-bit-memory access, three SBus expansion slots, and hold up to 256 Mbytes of system memory. Base systems start at $4000 and $5500, respectively, for 70- and 85-MHz boards. The SPARCengine 20 series target systems that need the multiprocessing horsepower of 60-MHz SuperSPARC+ modules. The model 612 combines two 60-MHz processor modules to deliver 88.9 SPECint92 and 102.8 SPECfp92 per CPU. In addition, two uniprocessor boards and a processor-less MBus motherboard also are available. The SPARCengine 20 motherboards include four 64-bit SBus slots, one or two 50-MHz MBus slots, space for up to 512 Mbytes of ECC memory, and 24-bit accelerated true-color imaging (opBAonal video SIMMs). Prices go from $5500 for the CPU-less motherboard to $10,800 for the dual-CPU version. Contact the SPARC Technology Business at (415) 336-0810.

The Solaris operating system's next release for SPARC, x86, and Pentium processors, Solaris 2.4, will be feature-for-feature-compatible with both Sparc and Intel-family platforms—and all derived from a single source base. Early versions of 2.4 were demonstrated last month by SunSoft, Mountain View, Calif., at the annual Solaris Developer Conference. Besides all of the features available in Solaris 2.3 for the Sparc and 2.1 versions for the x86, 2.4 provides a common application environment and tools to simplify system installation and management. Key new features include scalable symmetric multiprocessing support for up to 20-way multiprocessing systems, and an enhanced windows system with X11.R5 to support standard APIs. Other enhancements are standard libraries for 2D and 3D graphics, Adobe display postscript, a cache-file system, asynchronous point-to-point communications, multimedia support based on Live! (the Solaris resident software that includes an imaging library, software compression/decompression, and algorithm support for Group 3 and 4 faxes, full-motion video, MPEG, and h.261 formats). Solaris 2.4 will also pack C2-level security and networked system administration. General release will take place next quarter. Call SunSoft at (415) 336-1462.

▼ GUIDE HELPS PCMCIA DEVELOPERS



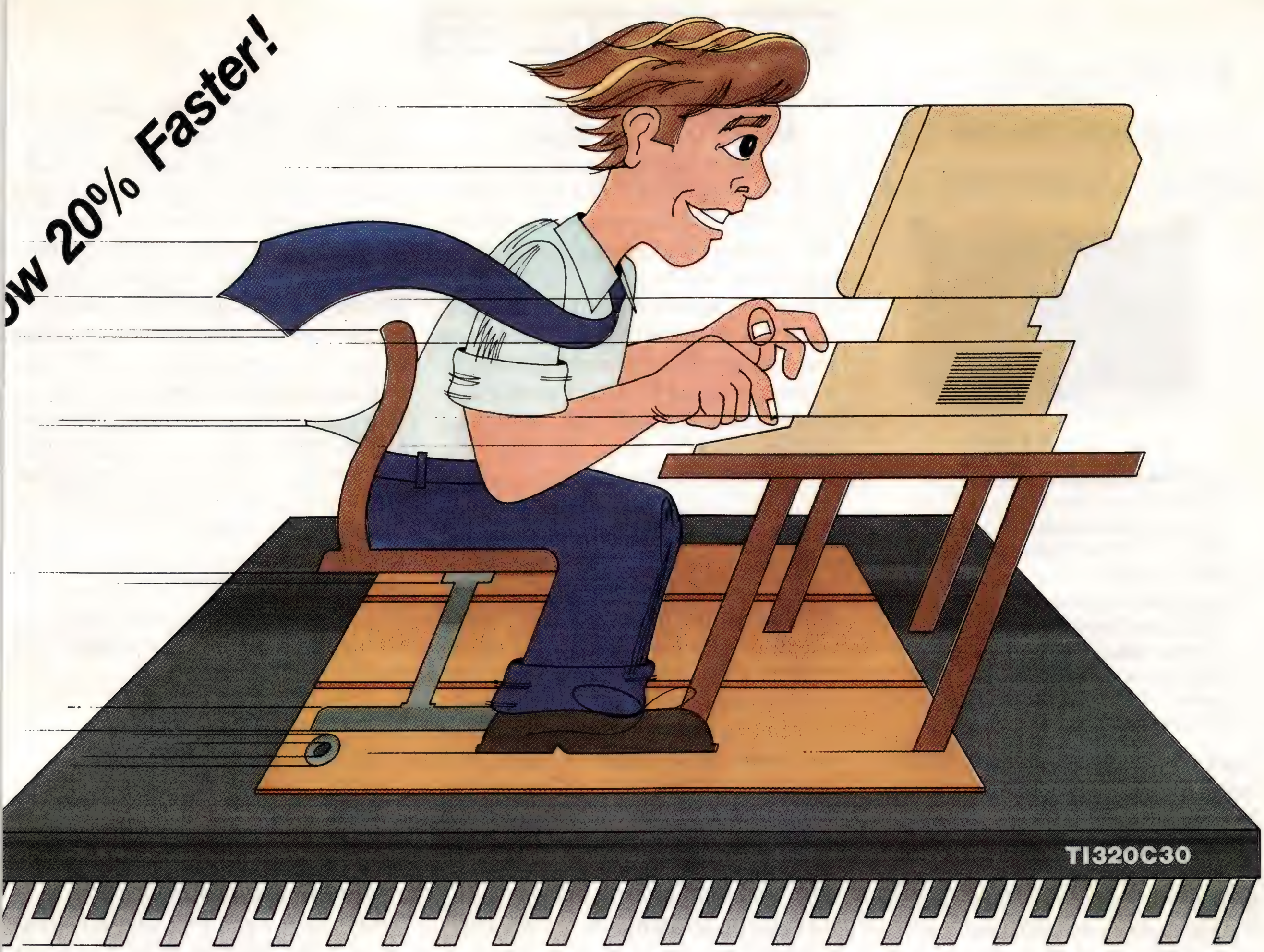
A comprehensive overview of the PCMCIA standard is given in the PCMCIA Developer's Guide. The text is supplemented with design examples, reference materials, and compatibility issues. Included is an extensive directory of PC Cards, host platforms, and desktop host adapters. An OEM directory supplies information on components, including ICs, development tools, and software. The guide is available now for $89.95.

Sycard Technology Inc.
651 Smoke Tree Way
Sunnyvale, CA 94086
(408) 247-0730
▶ CIRCLE 782

▼ 4X CD-ROM DRIVE SENDS 600 KBYTES/S

Double- and triple-speed CD-ROM drives are barely out of the chute. Now, a low-cost quadruple-speed drive is available with a data-transfer rate of 600 kbytes/s and an access time of 195 ms. The Super Quad, which comes with a 64-kbyte cache-memory buffer, is compatible with most industry standards, making it suitable for such applications as interactive multimedia, games, clip art, and photo archiving. Features of the drive include a motorized disk tray with an eject button, a front-panel headphone jack, and a rear-panel audio output for connection to sound boards. The Super Quad will be available in the third quarter for $399.

Teac America Inc.
7733 Telegraph Rd.
Montebello, CA 90640
(213) 726-0303
▶ CIRCLE 783



Beefed-up Banshee® II Blows Away Tough DSP Development Tasks

anshee, ASPI's popular system oard based on the Texas Instruments C30 Digital Signal Processor, ow has a big brother. The new anshee II boasts 4 Mbytes of zero ait-state static RAM and a speed ncrease to 40 MFLOPS.

Banshee II is available with shell, ASPI's powerful develop-ment environment that turns your rdinary AT into an exceptionally owerful DSP workstation. With Ashell, you spend your time working n the DSP problem instead of coping ith the computing environment.

Like its predecessor, Banshee II nchors a large family of interface oards and other devices; all are esigned to take full advantage of the Banshee II's flexible I/O and memory architecture. Data acquisition options include A-D/D-A, digital audio, and serial audio and serial voice interfaces.

Users who need to develop special interface boards will find this task simplified by host bus, 'C30 memory bus, and 'C30 I/O bus connectors on the Banshee II board. For detailed specifications and prices, contact

Atlanta Signal Processors, Inc.,
1375 Peachtree St. NE, Ste. 690
Atlanta, GA 30309-3115
404/892-7265/Fax 404/892-2512
Germany: MEDAV, (9131)583-0
Japan: Kobe Steel, 3(5634)5426

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WORLD LEADERS IN DSP DESIGN TOOLS

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1
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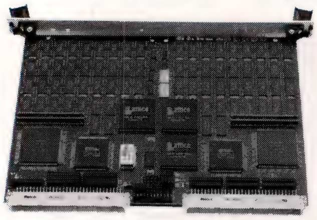
MEMORY MODULE
VME/VSB/VME64



CI-VME80

- Up to 80 Mbytes/Sec Transfer Rate on VME64
- Up to 40 Mbytes/Sec Transfer Rate on VME/VSB
- Fully Supports IEEE 1014 Rev.D & VSB Rev.C
- 32MB, 64MB, 128MB, 256MB, 512MB, & 1GB
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- Single Cycle times of 195ns
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- Access Times of 30ns Write/Read in Block Cycle
- Dual-Ported VME/VSB & VME64 in one 6U slot
- LIFETIME WARRANTY

The CI-VME80 is the ultimate memory board for VMEbus systems! Chrislin has designed the CI-VME80 with an onboard ALU to provide enhanced functionality for custom users. Available through AM codes are 64 bit arithmetic and logical functions (ADD, SUB, AND, OR, XOR) that will greatly enhance throughput in many applications. Simply write data to the location to be modified with the proper AM Code and the function is performed during the write cycle.

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Providing Top Quality Memory For Two Decades!

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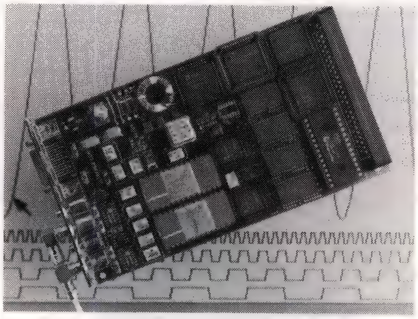
▼ PCMCIA CONTROLLER SPANS LOW VOLTAGES

A long-term upgrade path is offered with the VG-469 PCMCIA 2.1 ExCA controller. The chip supports current 5-V systems and emerging 3.3-V designs, and will be able to handle even lower voltages in the future. In addition, it's designed with a hardware mechanism that prevents damage to a lower-voltage PCMCIA card that's accidentally plugged into a higher-voltage socket. The chip supports both memory and I/O cards, as well as ATA solid-state and hard-disk drives. The chip also is compatible with the system bus timing of asynchronous and synchronous ISA and EISA architectures, including those based on the Intel 386SL microprocessor. The VG-469 can control two card sockets or be cascaded to control four sockets without any external logic. With external logic, the number of sockets is unlimited. By supporting mixed voltages, the chip's ISA bus and each of the two sockets can be independently operated at either 3.3 or 5 V. Other features include programmable power-management modes, individual socket-power control, and window-activity monitoring. The IC is housed in a 208-pin thin or plastic QFP and sells for under $15 in large quantities.

Vadem Inc.
1885 Lundy Ave., No. 201
San Jose, CA 95131
(408) 943-9301
▶CIRCLE 784

▼ SBUS BOARD ACQUIRES DUAL 5-MHZ CHANNELS



Two channels of analog information can be simultaneously acquired at speeds up 5 MHz using the ADDA1205DX board. The SBus-based board holds up to 16 Mbytes of dual-port RAM. In addition, while the 12-bit analog-to-digital data is streaming in, the board can sample four parallel TTL signals at the same 5-MHz rate and output four other TTL signals and two 12-bit analog signals. The board, which requires just one slot in the SBus system, is designed for scientific, medical, and industrial applications. The sampling rate is programmable from 200 ns to 51.15 µs per sample. Because the operate is done transparently, the CPU can tend to other tasks during operation. With a pipeline mode, all 16 Mbytes of DRAM can be used to input and output data. The user is simply required to fill the RAM with the desired data. A Unix driver and demonstration samples are bundled with the ADDA1205DX. The data-acquisition board sells for $4995. Slightly stripped-down versions are also available.

Ultraview Corp.
475 Yampa Way
Fremont, CA 94539
(510) 657-9501
▶CIRCLE 785

▼ VRAM ACCELERATOR HANDLES 64 BITS

Designed for the PCI and VL local buses, the Stealth 64 is a 64-bit VRAM-based graphics accelerator board. Based on the Vision 964 graphics engine from S3 Inc., the board accelerates Windows 3.1, AutoCAD, and other graphics applications by supplying true 64-bit pixel processing and VRAM access, and by offloading common graphics functions such as BitBLTs, rectangle fills, and raster operations from the system CPU. All color depths are fully accelerated to provide instantaneous screen updates, even in 24-bit true-color modes. With up to 4 Mbytes of VRAM and a 135-MHz RAM DAC, the board can display 65,536 colors at 1280 by 1024 pixels and true color at 1024 by 768 pixels. The Stealth 64 is built according to the DPMS standard for reduced energy consumption. Built-in utilities offer virtual desktop capabilities, including on-the-fly resolution switching. Available now, the Stealth 64 sells for $399 with 2 Mbytes of VRAM and $599 with 4 Mbytes.

Diamond Computer Systems Inc.
1130 East Arques Ave.
Sunnyvale, CA 94086
(408) 736-2000
▶CIRCLE 786

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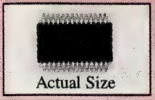
3.3V and 5V High Efficiency Dual Step Down Switching Regulator.

The LTC1142 dual-output ultra high-efficiency synchronous regulator controller, available in a compact 28-lead SSOP, maximizes battery life in a small amount of board space. The LTC1143 dual-output high-efficiency regulator controller is available in a space-saving narrow 16-lead SOIC package.


Actual Size

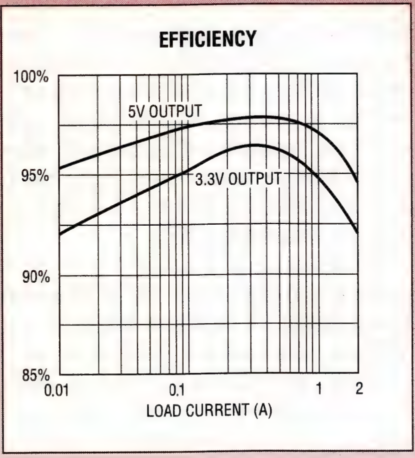
Both devices feature advanced Burst Mode™ power management circuity providing high efficiencies at load currents from a few milliamps to amps. Standby current is a low 160µA per regulator.

Both the LTC1142 and LTC1143 incorporate two independent regulator blocks providing 3.3V and 5V outputs with individual shutdown to less than 20µA. The LTC1142 operates over a 5V to 20V input range, allowing 10-12 cell battery packs.

The LTC1142 also supports full synchronous MOSFET switching for both regulator sections for efficiencies which can exceed 95%. The LTC1143 uses the fewest external components in the least amount of board space with efficiencies around 90%.

These versatile controllers also provide short circuit protection, very low dropout operation and excellent transient response. Pricing starts at $ 5.45 in 1000 piece quantities for the LTC1143CS.

For more details, contact Linear Technology Corporation, 1630 McCarthy Boulevard, Milpitas, California 95035/ 408-432-1900. For literature only, call **1-800-4-LINEAR.**



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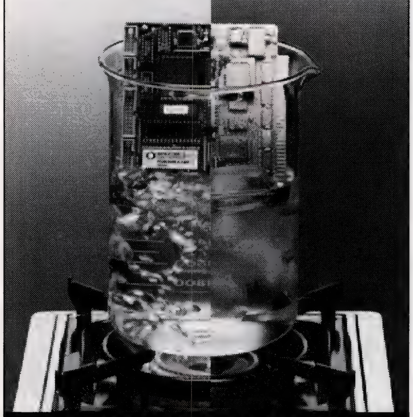

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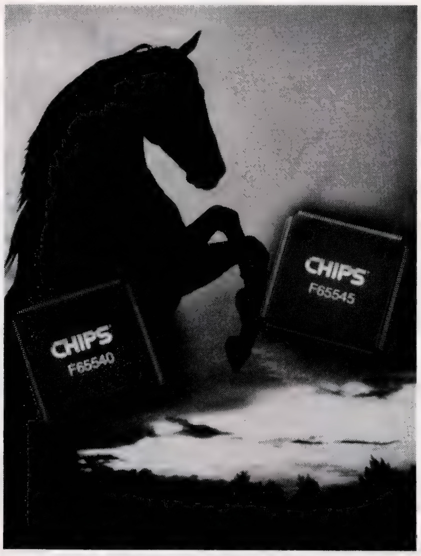
▼ GET DESKTOP PERFORMANCE ON A FLAT-PANEL DISPLAY

Desktop graphics performance is possible on a flat-panel LCD using the Mustang family of controllers. By including video-overlay capability, OEMs can add television sources and video input to a portable system from a camcorder, laser disk, or other NTSC/PAL input. The family consists of two parts—the 65540 and 65545.



The two controllers are software- and pin-compatible, and they share a common feature set as well as support most panel types. The 65545 adds an integrated hardware accelerator for increased performance. Both parts incorporate a VGA flat-panel and CRT controller; a true-color, 24-bit/pixel digital-to-analog converter; a programmable clock synthesizer; current-reference and comparator logic; and a video-input port. A direct interface to the VL-Bus local bus is incorporated.

Power-saving features are integrated and the controllers can run from either 3.3 or 5 V. A BIOS that's VGA-compatible is included, as well as software drivers for the Windows, Windows NT, and OS/2 operating systems. The 65540 is available now for $24 in large quantities. The 65545 will sample in July, with production starting in September. It will be priced at $31, also in large quantities.

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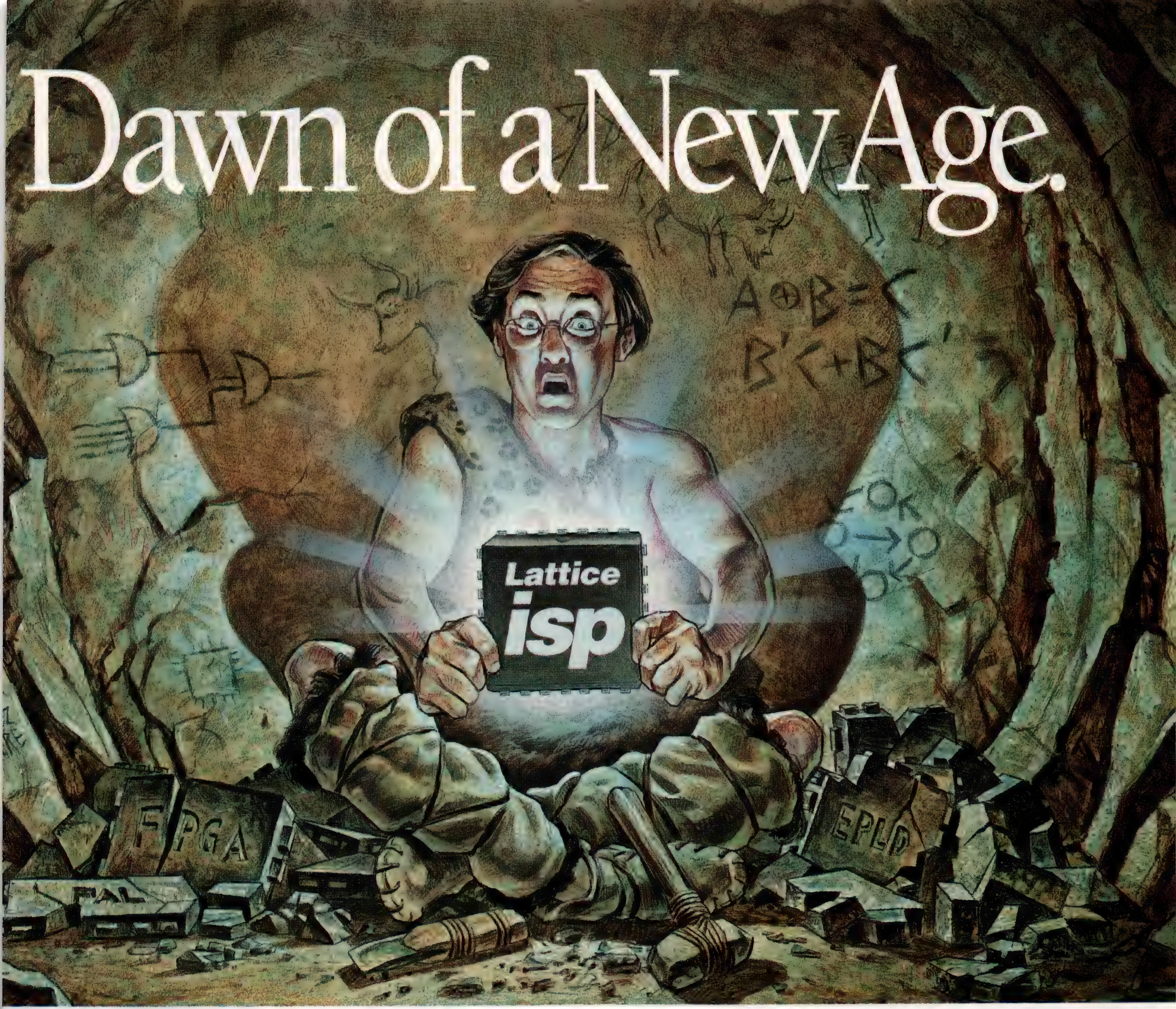

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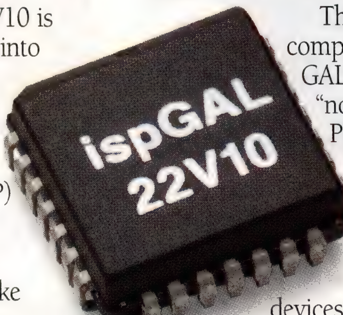

The ispGAL22V10 is fully compatible with the popular GAL22V10 device. It utilizes the "no-connect" pins of the 28-pin PLCC GAL22V10 pin-out for the ISP control signals—making the devices footprint compatible. And the serial ISP interface lets you daisy-chain any number of devices for simple programming.

Discover the power of Lattice's new ispGAL22V10. Call **1-800-327-8425** or FAX 503-681-3037 today for a **free ispGAL22V10 sample** and data sheet. Ask for information packet 319.

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SYSTEM DESIGN PRODUCTS

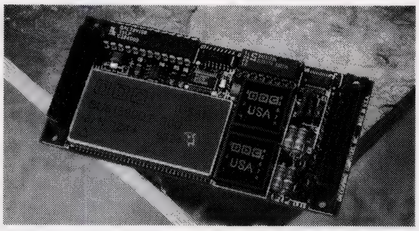
▼ DEVELOPER'S KIT SIMPLIFIES MPEG DESIGNS

An MPEG video-playback development kit enables board and system designers to build low-cost CD video platforms. The kit includes a reference design that employs three playback chips: the AuraVision VxP500, the C-Cube CL450, and the Texas Instruments AV110. It also comes with a royalty-free software license for source and object code, along with an open APR+I for titles and games development. Both DOS and Windows environments are supported. A key feature of the reference design is its ability to supply full-motion, full-screen video playback, along with hardware acceleration of AVI video, such as Indeo, Cinepak, and Video 1. Available now, the developer's kit will let designers build a board for less than $145.

AuraVision Corp.
47865 Fremont Blvd.
Fremont, CA 94538
(510) 440-7180
▶CIRCLE 788

▼ MEZZANINE MODULE ADDS 1553 SUPPORT

A 1553 interface module has been added to the family of IndustryPack mezzanine bus boards. Dubbed the IP-1553, the board forms a complete dual-redundant MIL-STD-1553B bus terminal. Complete multiprotocol support of 1553B as a bus controller, remote terminal, and bus monitor is supplied. Support is included for both direct- and transformer-coupled interfacing to the 1553 bus cable. The module ships with a C library. It sells for $2995.



GreenSpring Computers Inc.
1204 O'Brien Dr.
Menlo Park, CA 94025
(415) 327-1200
▶CIRCLE 789

▼ CD-ROM DRIVES SUPPORT INDUSTRY STANDARDS

Support for most industry standards is bundled with the RRD44 CD-ROM drive. This includes CD-ROM XA, MultiSession, PhotoCD, MPC 1 and 2, CD-DA, and CD-I. As a result, the high-performance drive is suited for such applications as multimedia, video, and networking. A lower-performance and -cost version, the RRD43, also is available.

The average access time of the RRD43 is 320 ms, while the RRD44 lowers that time to 200 ms. The cache memory on the lower-cost model is 64 kbytes; the high-end version holds 256 kbytes. Firmware that's resident in both units tunes them for DEC systems, simplifying integration and offering the ability to boot from the CD-ROM drive. Prices for the drives start at $340.

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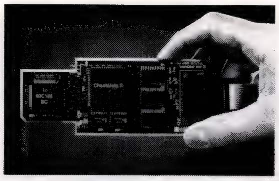

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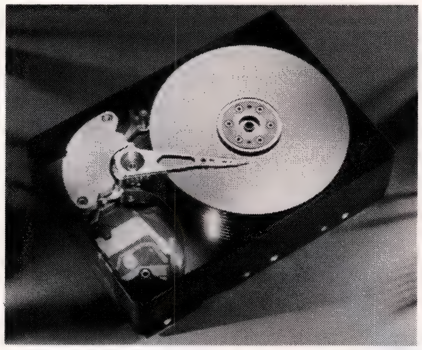
▼ 4-GBYTE DRIVE SPINS AT 7200 RPM

The capacity levels of hard-disk drives continue to rise, as is evidenced by the Grand Prix 4280. The 4-Gbyte 3.5-in. drive uses a 7200-rpm rate to transfer data at 9.7 Mbytes/s, thus internally producing an average latency of 3.3 ms. The average seek time is 8.6 ms. High-performance is partly due to the drive's PRML (partial response, maximum likelihood) capability. The PRML read channel increases the areal density by 30% to 40% over competitive products. The drive can transfer 20 Mbytes/s externally through a fast and wide SCSI-2 interface. It sells for $2500, while a 2-Gbyte version goes for $1650. Samples are available now. Volume production will start in the third quarter.



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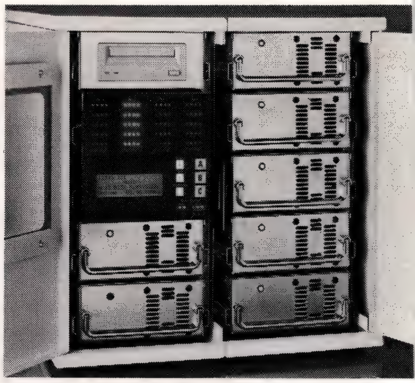
▼ RAID ENCLOSURE HOLDS 20 DRIVES

The RD35 is an application-ready intelligent enclosure for RAID subsystems, which gives integrators a housing that's ready to support RAID levels 0, 3, and 5. The product is certified to run with most Unix-based platforms, including DEC, HP, Sun, and IBM. The housing has room for up to 20 3.5-in. disk drives, offering a capacity of up to 32 Gbytes. Other features include read-through and write-back cache memory (up to 128 Mbytes) and full redundancy to critical components. The system's downtime is checked through the enclosure's drive caddies, which allow users to hot-swap a failed component. It also offers an on-board RS232 port and LCD panel, letting users monitor system performance. Up to three bays can be tiered for further expansion. Prices for the RD35 start at $7500.



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BENCHTOP DSO FEATURES FULL AUTORANGING

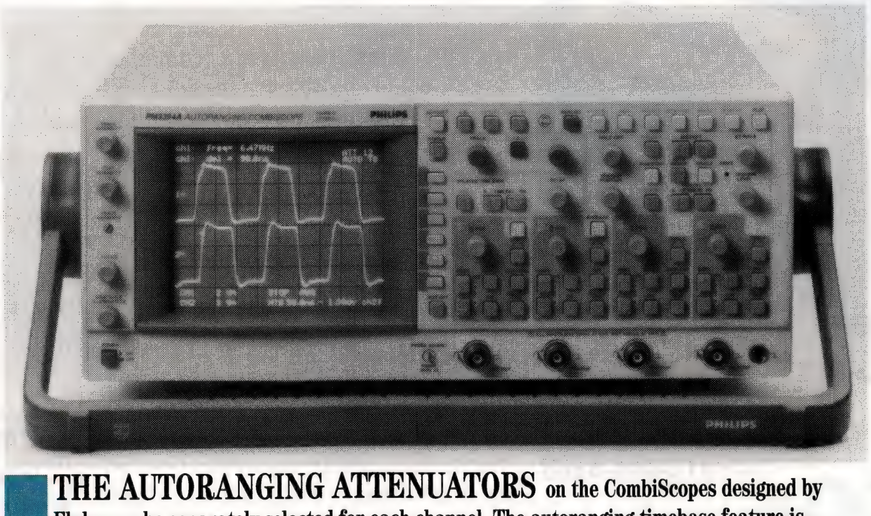
A DIGITAL AND ANALOG OSCILLOSCOPE AUTOMATICALLY VARIES ATTENUATION AND TIMEBASE TO TRACK CHANGING SIGNALS.

JOHN NOVELLINO

Designers troubleshooting their prototypes typically keep one hand on their oscilloscope probe, which frequently moves around. The other hand must remain free to manually set the attenuator and timebase controls, which also move around frequently as the probe jumps from point to point. Although most designers get pretty adept at this manual hopscotch, they would rather avoid such movement during troubleshooting.

The latest series of CombiScopes developed by Fluke Corp. do just that. The instruments (named for the fact that they incorporate a digital and analog oscilloscope in one instrument) introduce autoranging capability to the area of benchtop/portable oscilloscopes. The autoranging feature makes the needed attenuation and timebase changes as the probe moves from one point to another, with no action on the part of the user. The oscilloscopes also offer a true variable timebase as well as autotracking phase measurements.

Four models make up the new series of CombiScopes. Two four-channel models, the PM 3384A and PM 3394A, have 100- and 200-MHz bandwidths, respectively *(see the figure)*. The PM 3382A and PM 3392A have similar bandwidths, but are configured as "2+2"-channel oscilloscopes, in which the third and fourth channels are attenuated only at 0.1 V/div. and 0.5 V/div.



THE AUTORANGING ATTENUATORS on the CombiScopes designed by Fluke can be separately selected for each channel. The autoranging timebase feature is independently selected with another button push.

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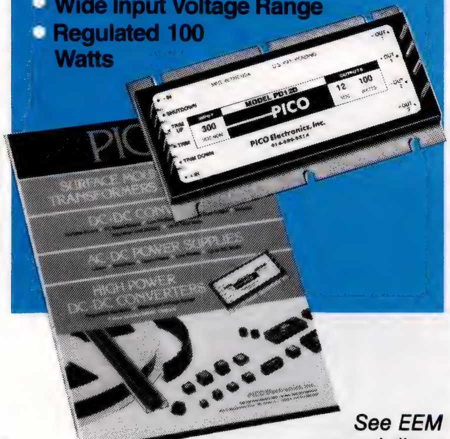

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READERS SERVICE 170

Sampling speed for the digital side is 200 Msamples/s at 8 bits on one channel, and 100 Msamples/s on two channels. Record length is 8 ksamples (32 ksamples optional).

Autoranging operates differently than the autoset feature, which works once with each push of the appropriate button. Autoranging operates continuously to maintain an optimum display as the input signal changes. Users can select the autoranging attenuators, which are independent of the autoranging timebase, separately for each channel. The attenuators keep the signal display between two and six vertical divisions, using the normal 1-2-5 steps. When two channels are shown, a special window display mode keeps the traces in their allocated areas to ensure a clear, nonoverlapping view of each while maintaining high vertical resolution for detailed measurements.

The autoranging timebase can operate in two ways. In the "steps mode," this feature again uses the normal 1-2-5 timebase steps. As with the autoranging attenuators, this mode is useful when the user probes unknown signals, makes circuit adjustments, or changes the circuit's input in a way that affects its output. If the adjustment is too large, autoranging brings the signal back on screen, where automatic parameter measurements can be made.

Autoranging also uses the instrument's variable timebase. With this feature selected, the oscilloscope will maintain the same number of periods or part of a period on the display despite changes in the signal's frequency. This capability comes in handy when circuits are tested at different frequencies or in mechanical applications that test machines at different speeds.

The truly variable timebase in the new oscilloscopes isn't based on a rescaling of the display, which reduces horizontal resolution and slows the update rate. The system employs a proprietary sampling technique in which the clock frequency is programmable in very small increments, rather than in the traditional 1-2-5 steps. As a result, the digital oscilloscope's timebase acts similar to that of an analog oscilloscope.

Besides its inherent usefulness, the signal-tracking capability of the latest CombiScopes allows the instruments to make automatic phase measurements with the cursors. The cursor phase-measuring mode automatically sets the cursor reference to one signal period. If the frequency changes, the oscilloscope tracks the change without any user intervention. In addition, the cursors can isolate part of the trace for other measurements or mathematical manipulations.

As with the earlier CombiScopes, the new series has an extensive set of built-in automated measurements. Measurements can be initiated from a button mounted on the probe as well as from the front panel. The Math+ option adds integration, differentiation, histogram, and fast-Fourier-transform calculations, along with pass-fail testing on either signal envelopes or measurement results.

To make sure that all of these automated functions don't bog down throughput, the oscilloscopes incorporate three processors. As a result, autoranging corrects the display faster than a user can move his eye from the new test point to the screen.

Advanced trigger modes include logic state, pattern, and glitch triggering (down to 2 ns). In addition to pre- and post-trigger display, the oscilloscopes provide event-delayand time-after-event delay capability. TV triggering and a built-in line counter are included, as are a real-time clock, date- and time-stamping, and hardcopy and acquisition functions.

The oscilloscopes come with a serial interface for hard-copy output and PC communication. An optional IEEE-488.2 interface is compatible with the Standard Commands for Programmable Language. ☐

PRICE AND AVAILABILITY

The PM 3382A, PM 3384A, PM 3392A, and PM 3394A go for $5175, $5675, $6175, and $6675, respectively. The math option, the IEEE-488.2 interface, and an extended memory each cost $515. Delivery is three weeks after receipt of an order.

Fluke Corp., P. O. Box 9090, Everett, WA 98206-9090; (800) 443-5853 or (206) 347-6100.

CIRCLE 513

HOW VALUABLE?	CIRCLE
HIGHLY	533
MODERATELY	534
SLIGHTLY	535

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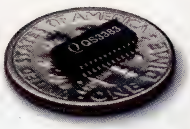

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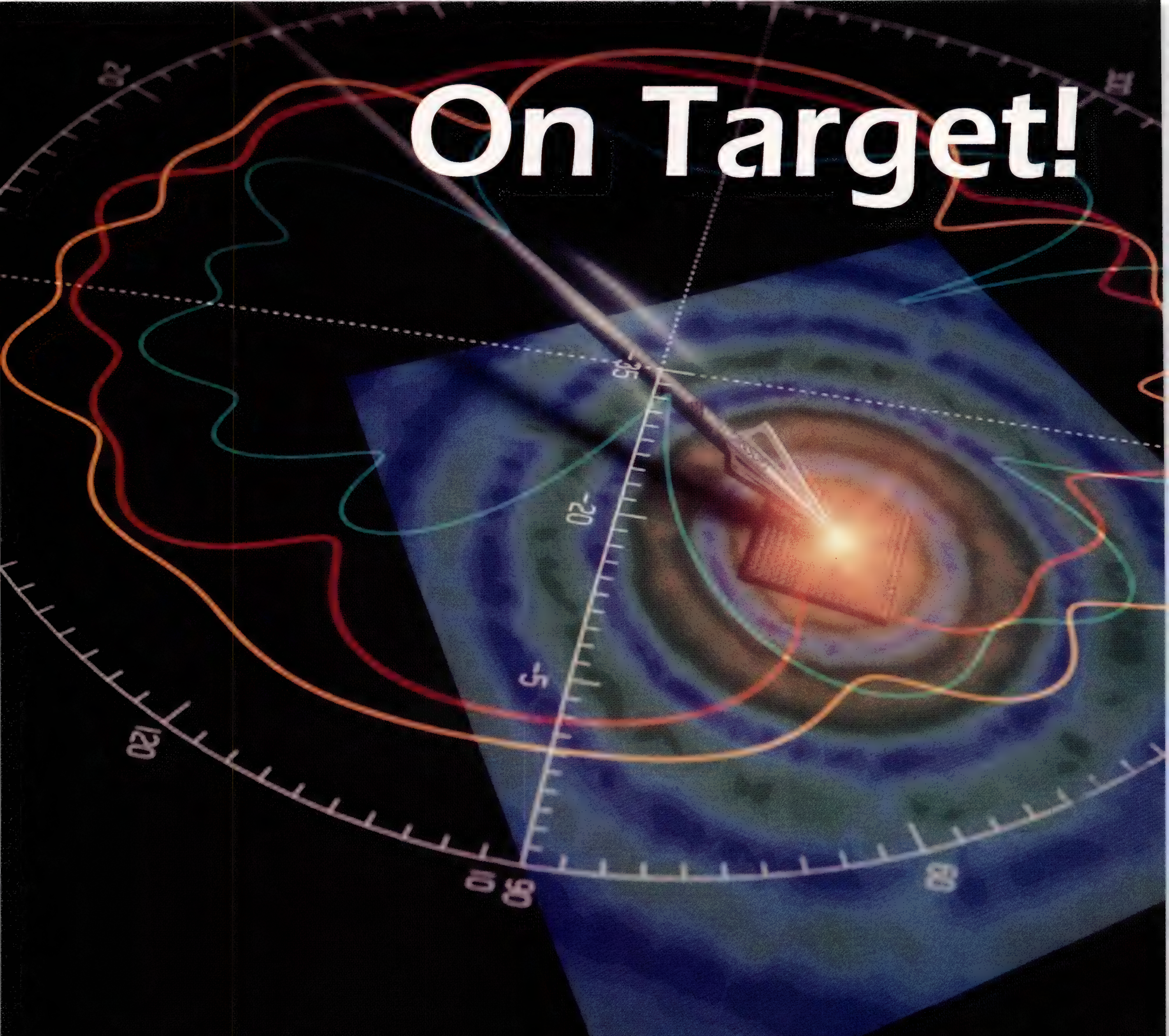

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PARALLEL PROCESSOR PUTS OUT 2.56 BILLION MACS

A PC-BASED BOARD THAT'S COMPARABLE TO A WORKSTATION HOLDS UP TO 128 PROCESSORS, ACCELERATING PATTERN-RECOGNITION ALGORITHMS.

RICHARD NASS

Engineers who typically run any type of compute-intensive analyses on PCs are continually frustrated by the scarcity of high-performance processing boards. High-end prcessing boards tend to find homes in a VMEbus, Multibus, or a similar-performance platform. Those that do happen to fit the AT form factor are usually quite pricey.

In trying to fill that void, Adaptive Solutions Inc. came up with the CNAPS/PC (Coprocessing Node Architecture for Parallel Systems/PC). This architecture essentially gives PC users the same performance level on their desktop computers as their workstation-running colleagues. The parallel-processing board holds one or two CNAPS-1064 parallel-processor CPU chips for a maximum of 128 processors *(Fig. 1)*.

The board can perform 2.56 billion multiply-accumulate operations/s (MACS). This performance level is suitable for such applications as real-time-speech and optical character recognition; neural networks; and forms, image, and signal processing. Typically, the computationally-intensive data contained in these applications is multifaceted and naturally parallel. It does require a real-time compute engine, however.

Similar to a math coprocessor or a graphics coprocessor, the CNAPS/PC board offloads pattern-recognition tasks from the host-computer CPU. Its architecture is general enough that it allows it to handle a wide span of applications ranging from medical diagnostics to manufacturing process control.

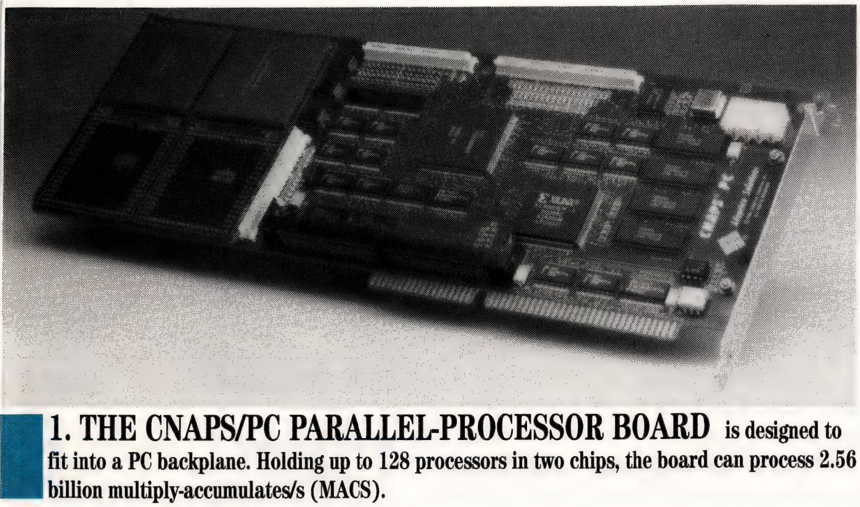
FULL-SIZE PC BOARDS

The board is a full-length AT board containing either one or two microprocessor chips, on-chip memory, as well as an ASIC sequencer (instruction unit) *(Fig. 2)*. Data moves at a rate of 80 Mbytes/s through an Adaptive Solutions external port. With its mezzanine-board capability, the CNAPS/PC can be expanded to 384 processors and 7.68 billion MACS.

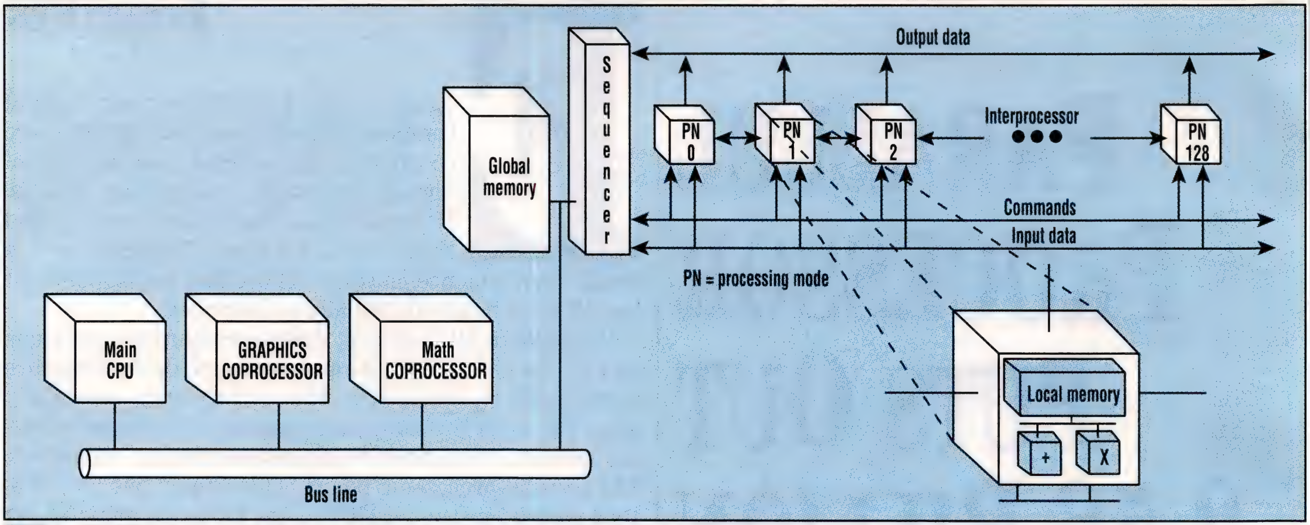
The CNAPS-1064 massively parallel microprocessor, which runs at a clock frequency of 20 MHz, contains 16 or 64 processors on one chip. Each CNAPS chip contains 14 million transistors, 11 million of which are active.

When manufacturing a CNAPS chip, Adaptive Solutions places 80 processors on each chip. However, only about 80% of the transistors (64) on the chip are activated. This is sufficient to ensure high process yield levels, thus lowering chip cost.

Each processing node (PN) in the chip is actually a complete fixed-point arithmetic processor that can perform 1-, 8-, and 16-bit calculations. The CPU, which is a CMOS chip manufactured on a 0.8-μm two-metal process, is housed in a



1. THE CNAPS/PC PARALLEL-PROCESSOR BOARD is designed to fit into a PC backplane. Holding up to 128 processors in two chips, the board can process 2.56 billion multiply-accumulates/s (MACS).



2. THE PARALLLEL-PROCESSOR BOARD PASSES DATA **between the global memory and the individual processors through a data sequencer. Each processing node is scalable up to 128 processors.**

106-pin ceramic PGA package. The chip's bare die is quite small and measures 1 in.^{2}.

SIMD OPERATIONS

The CNAPS processors are configured to operate on data for single-instruction, multiple-data (SIMD) execution. The SIMD architecture allows for a straightforward single-threaded programming model.

This SIMD architecture offers several advantages. It actually eliminates the caching and pipelining needed to feed each processor and data from memory.

Each processor on the chip is a complete digital-signal processor with its own 4-kbyte on-chip data memory. Consequently, an entire set of data computations can be carried out in one clock cycle. Furthermore, it's possible to incorporate up to 32 Mbytes of RAM into the board using standard SIMMs.

The sequencer ASIC broadcasts input data and a PN local-data value to every PN in the array. All activated PNs execute the same instruction in unison on the data element, but different data is presented to each processor. Because of this parallel operation, an entire set of data computations can be carried out in just a single step.

This architecture was chosen because most of the pattern-recognition algorithms employed in speech-, character-, and image-recognition systems can be divided in such a manner.

PROGRAMMABILITY

The CNAPS architecture is designed to be programmable and to run different types of algorithms for preprocessing, classification, and post-processing, all performed on the same hardware.

In addition, the CNAPS architecture is scalable. That means users can choose precisely how many processors they need to dedicate to a particular application.

A comprehensive development environment is available and comes bundled with the CNAPS/PC parallel-processing board. As a result, software programmers can develop custom applications, or use the precoded algorithms to run experiments without doing any programming.

The software-development tools are many. They include CNAPS-C; CPL; BuildNet, a source-level debugger; and various application libraries that each of which contain callable functions.

PARALLEL COMPILER

CNAPS-C is a specialized parallel C compiler for writing custom algorithms. It offers several extensions to the C language to support parallel-programming tasks of the CNAPS array and CNAPS fixed-point arithmetic.

CPL is an assembler that helps developers write custom algorithms and implement them in an application. The CPL offers complete control over the hardware and produces the most efficient and compact software code.

BuildNet offers fast, straightforward access to the board through any of three user interfaces_graphical, command-line, or C. It also offers straightforward access to the board through a set of prewritten neural-network algorithms. Little programming experience is needed because the algorithms are precoded and ready to run.

Since the processors run at a relatively slow speed with a clock frequency of 20 MHz, power consumption is just 4 W per chip. This, in turn, keeps the heat dissipation down. The clock speed also makes it possible to use off-the-shelf memory, rather than proprietary DRAM, further reducing the cost. ☐

PRICE AND AVAILABILITY

The CNAPS/PC comes with 16, 32, 64, or 128 processors. The boards sell for $2995, $3995, $4995, and $6995 each, respectively. Large-quantity discounts are available. All versions are due out by July. In addition, the company offers a VMEbus version with 256 processors.

Adaptive Solutions Inc., 1400 N.W. Compton Dr., Suite 340, Beaverton, OR 97006; (503) 690-1236. **CIRCLE 512**

HOW VALUABLE?	CIRCLE
HIGHLY	527
MODERATELY	528
SLIGHTLY	529

PRODUCTS NEWSLETTER

COMPLEX PLD OPTIMIZED FOR PCI BUS AND JTAG

Banking on its combination of flash-memory technology and SRAM configuration cells, designers at Intel Corp., Folsom, Calif., enhanced their high-complexity programmable-logic family with the iFX8160, the first programmable device to include an interface optimized for the peripheral-component-interconnect (PCI) bus. The 120 on-chip buffers can directly drive the PCI bus, permitting the Flex chip to connect directly to the bus. The chip also permits in-circuit reprogramming and logic partitioning for on-the-fly reprogramming of only one portion of the array at a given time.

The in-system reconfiguration is possible thanks to the use of the chip's JTAG serial scan test port. Resources on the chip include 160 macrocells arranged in 16 configurable function blocks (CFBs). Each CFB can serve as either a 10-ns block of 24V10-like logic, or as 128-word-by-10-bit 15-ns SRAM. When operating, the chip draws 2.5 mA/MHz from a 5-V supply, but just 5 μW during standby. The chip comes in a 208-lead PQFP and is supported by the latest release of the company's PLDshell Plus V4.0 design software. In lots of 1000 units, the 10-ns version sells for $119 each; a 12-ns version sells for $99. *DB* **CIRCLE 905**

SPEED UPGRADES PUSH OPERATION TO 143 MHZ

Even though it just released its Flash370 family of CPLDs, designers at Cypress Semiconductor Corp., San Jose, Calif., have already upped the maximum operating speed. The CY7C371, a 32-macrocell chip, now has a top operating speed of 143 MHz when tested using the PREP benchmarks in benchmark suite 1, version 1.3. Overall, the CY7C371 rated almost 15% higher in average internal frequency than most competitive devices across all nine benchmark configurations. *DB* **CIRCLE 906**

HYPERSPARC MBUS CARDS UP CPU CLOCK TO 66 MHZ

Offering designers the opportunity to upgrade their MBus-based SPARCstation 10 desktop computers, or the SPARCserver 600 servers, a speed upgrade of the HyperSPARC MBus CPU card from Ross Technologies Inc., Austin, Texas, lets older systems push their operating clock speeds to 66 MHz. That represents a boost of about 20% over Ross's previously available 55-MHz MBus CPU cards. The higher-speed CPU cards occupy one MBus slot and lets the systems they're plugged into deliver about 20% higher throughput—upping the performance to 67 SPECint92 and 87SPECfp92 for a single-CPU module. Dual and Quad processor versions of the 66-MHz CPU card are also available. On average, these HyperSPARC upgrades to the original CPU supplied with the systems deliver two to four times the throughput when running Solaris 1.1 or release 2.3. On top of the enhanced-speed CPU cards, which cost $3490, $6380, and $11,960, for the single-, dual-, and quad-processor versions, respectively, prices for the 55-MHz versions of the HyperSPARC MBus cards were reduced by about 20% to $2760, $4760, and $7960, respectively. Each upgrade card comes with a software CD-ROM disk and a new boot-PROM for installation in the host system. Call Steve Goldstein, (512) 892-7802, x. 519. *DB* **CIRCLE 907**

LOW-POWER PROCESSOR TARGETS COMMUNICATIONS

Running at up to 25 MHz on 110 mW of 3.3-V power, the RUBY advanced communication processor from VLSI, San Fernando, Calif., has an architecture that's optimized for portable-communications applications, such as CDPD, wireless LAN, and modem products. Sporting a diverse assortment of I/O interfaces, the processor contains a UART, an 8-bit PIO, a high-speed serial port, and a FIFO-buffered PCMCIA/ISA interface, which can be configured for I/O, memory, or communications applications. The chip also provides an on-chip 512-by-32 SRAM, three timers, and an interrupt controller. External I/O or memory may be interfaced directly through a buffered bus, which accommodates 8-, 16-, or 32-bit data. At the heart of the RUBY processor is the ARM CPU, a powerful 32-bit RISC-based processor developed by ARM technology and licensed as to VLSI for use as a logic core in it's cell library. The innovative architecture and power-management features of the ARM processor give RUBY extremely high performance and low power consumption. A large suite of available development tools include a C-compiler, assembler, simulator, operating systems (including a graphical debugger), and development cards for UNIX and PC platforms. Samples are available in a 176-pin TQFP package, with full production scheduled for October. Pricing is $31.90 in lots of 10,000. *LG* **CIRCLE 908**

Edited by Clifford Meth

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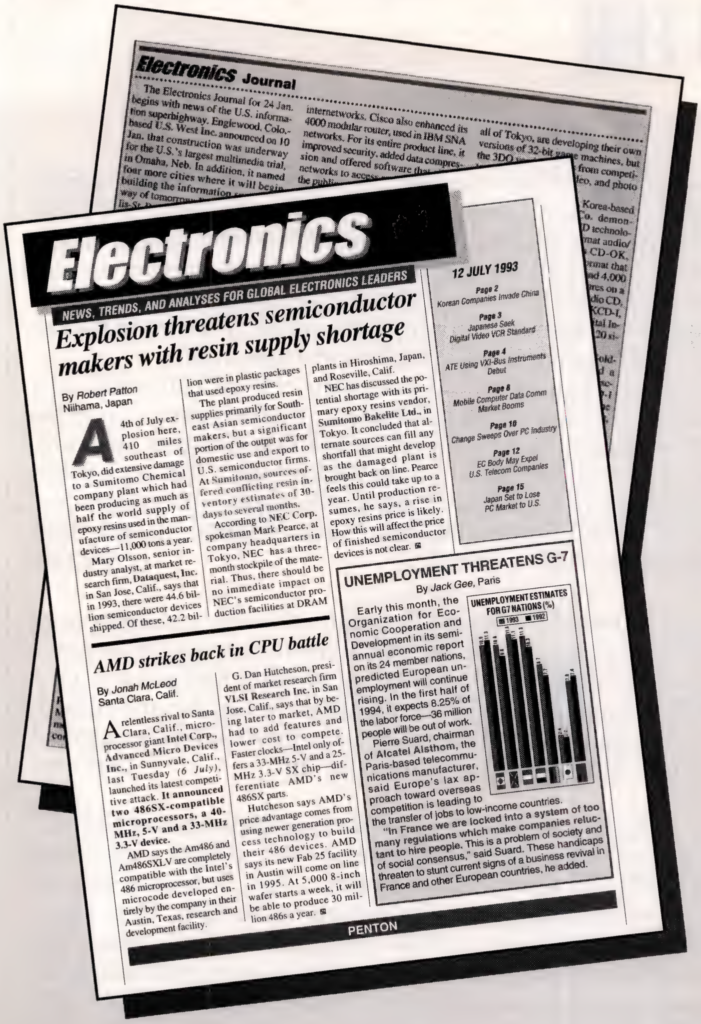

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

internetworks. Cisco also enhanced its 4000 modular router, used in IBM SNA networks. For its entire product line, it improved security, added data compression and offered software that

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

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Japan Set to Lose PC Market to U.S.

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.**, in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear. ■

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp.**, **Advanced Micro Devices Inc.**, in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year. ■

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of Alcatel Alsthom, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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ENHANCED HYPERSPARCS OPERATE AT 110 MHZ

Through a combination of improved CMOS fabrication technology and the use of multi-die packaging, a new family of hyperSPARC-based MBus CPU modules and 131-lead pin-grid-array packages give designers access to the highest-performance Sparc-compatible processors to date. Developed by the Ross Technologies Div. of Fujitsu, the enhanced Sparc CPU and cache subsystem included on the MBus module employs a 3.3-V half-micron CMOS process that uses three-levels of metal interconnections.

The result of that process are very small, low-power, fast chips that let designers build Sparc-compatible systems that can now run at 80, 90, and 100 MHz, with a 110-MHz version available in July. At 100 MHz, the hyperSPARC CPU delivers a throughput of 111 SPECint92 and 135 SPECfp92. Those numbers represent about a 50% improvement over the previous family of MBus modules.

Part of the speed improvement is the use of a higher-density packaging technology, which places multiple chips on a either silicon substrate, or on a copper/polyimide substrate. The silicon version is supplied by N-Chip Corp., San Jose, Calif., and the copper/polyimide version was developed by Fujitsu. Both cost the same and are qualified to deliver identical performance at the board level. The multichip packaging reduces chip-to-chip delays, trims parasitic losses, and lets the chip set (the CPU and memory subsystem) operate much faster than the previous generation, which used tape-automated bonding for each chip and mounted the TAB packages on the circuit board.

In addition, the reduced supply voltage allows the new chips to deliver their higher performance, yet not dissipate more power than the previous-generation MBus card. Thus, system designers do not have to make any power supply or power-busing changes to take advantage of the upgrade. There will be three versions of the MBus module—the RT6221, 6224, and 6226, with the 6221 containing a single hyperSPARC CPU with 128 kbytes of cache, the 6224 doubling the cache, and the 6226 providing the equivalent of two 6224s on one card.

For designers that need the ultimate in density, Ross will also offer the multichip assembly in a 131-lead PGA package. This solution is ideal for high-performance I/O processors, servers, and other custom-designed systems that don't necessarily run the workstation software. Two versions of the multichip PGA will be available, the RT628 and 629, with the 628 packing 128 kbytes of cache, and the 629 offering 256 kbytes.

The MBus modules are immediately available in 80-, 90-, and 100-MHz speed grades for new system designs. Prices in sample quantities of 1 to 10 units for the RT6224 (single CPU, 256 kbytes of cache, 40-MHz MBus interface) start at $2511, $3187, and $4019, each, respectively, for the three speed grades. An end-user upgrade kit using these modules will be available later this year, which will include the MBus card, a CD ROM, and a new boot PROM to provide the operating system upgrade information.

***Ross Technologies Inc.,** 5316 Highway 290 W, Ste. 500, Austin, TX 78735-8930; Steve Goldstein, (512) 892-7802 ext. 519.* CIRCLE 800

■ *DAVE BURSKY*

RECONFIGURABLE FPGAS PACK 2K-5K USABLE GATES

SRAM-based field-programmable gate arrays are reaching new levels of flexibility with the availability of the AT6002 and 6005, in-system reconfigurable chips with 2000 and 5000 usable gates, respectively. The arrays' architecture offers thousands of registers for pipelining, toggle rates of 250 MHz for on-chip logic, and guaranteed clock skews of less than 1 ns across the chips. Fabricated with a CMOS SRAM process, the chips draw little current during standby (500 μA)—less than most FPGAs. In addition to general in-system programmability, the AT6002 and 6005 incorporate the company's Cache Logic capability, so the chip can either be fully or partially reconfigured on-the-fly, without losing register data or disrupting logic, clocks, and I/O functions to the rest of the chip. One chip can actually do the work of several in the system by just uploading the desired logic patterns to a portion of the chip while the system is running. Other SRAM-based FPGA families require chips to be totally reset and reloaded with the new configuration pattern, slowing down overall system operation.

The internal structure of the arrays consists of a "checkerboard" of 64 cell sectors, with each sector containing a group of identical logic cells. The array core is surrounded by the I/O cells. All the cells are interconnected by local and express buses—special repeaters are included within the array to provide signal transfer points and signal regeneration. Each logic cell can be configured in many options, providing functions such as XOR/NAND, multiplexer, register, three-state, and wire. Propagation delays in the cell are 1.2 ns, when implementing a wire, to 2.2 ns for a NAND, and 2.4 ns for an XOR function. I/O buffers can handle loads of 12 mA and have propagation delays 1.2 ns as an input buffer; 3.5 ns as an output buffer. The AT6002 includes 2000 usable gates, 1024 (maximum) registers, 96 I/O lines, and typically consumes about 30 mA. Packing 3136 registers, the 5000-gate AT6005 provides 108 I/O lines and draws about 80 mA from a 5-V supply. The chips will come in thin quad-sided flat packages, and with 2- or 4-ns logic delays. In lots of 5000, the AT6002 and 6005 cost $16 and $72 each in PLCC packages.

***Atmel Corp.,** 2125 O'Nel Dr., San Jose, CA 95131; Joel Rosenberg, (408) 441-0311.* CIRCLE 801

■ *DAVE BURSKY*

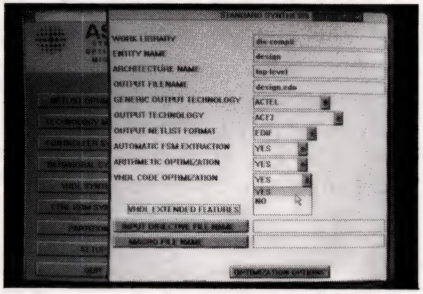
LOGIC-SYNTHESIS TECHNOLOGY TARGETS COMPLEX PLDS, FPGAS, AND ASICS

The ASYL+ logic-synthesis tool from Innovative Synthesis Technologies (IST) targets three different device technologies—complex PLDs, FPGAs, and gate-array and standard-cell ASICs. ASYL+ is a VHDL-based system that runs on both PCs and Unix workstations.

The tool accepts Palasm, ABEL, and VHDL inputs. Users have the benefit of efficient calls to library macros, parameterized generators, and user-defined blocks. These capabilities are important in FPGA design because engineers don't have to re-synthesize arithmetic blocks, but can instead use the FPGA vendors' pre-designed blocks.

ASYL+ has strong state encoding options for state-machine design, which is often a critical design parameter. Encoding options include one-hot, sequential, Gray, Johnson, random, and compact. Compact encoding exploits a IST-developed algorithm that improves area utilization by 30%.

At the low end of the design hierarchy, ASYL+ incorporates technology-dependent mappers that are optimized for each of the three types of target devices. Package partitioning extended to FPGAs lets ASYL+ synthesize and partition large designs for prototyping, or divide end products among several packages within a technology or across technologies. Because the tool is based on a functional approach, critical path containment and respect of the hierarchy are guaranteed. In addition, technology migration capabilities are not restricted to glue logic or gate net-list migration, but include library macroblocks and parameterized generator transfers from any one technology to another.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GENERIC OUTPUT TECHNOLOGY ACTEL
OUTPUT TECHNOLOGY ACT1
OUTPUT NETLIST FORMAT EDIF
AUTOMATIC FSM EXTRACTION YES
ARITHMETIC OPTIMIZATION YES
VHDL CODE OPTIMIZATION YES

The ASYL+ software runs on PCs and Sun workstations, and is shipping now. Pricing for the PC version of the synthesis engine and one library starts at $2800. Typically, a complete PC-based ASYL+ design system, consisting of VHDL support, multi-technology partitioning and targeting, and three device mappers, goes for $15,500.

Innovative Synthesis Technologies California Inc., *P.O. Box 1897, Danville, CA 94526; (510) 736-2302.* **CIRCLE 802**

■ *LISA MALINIAK*

VHDL TOOL MODELS ANALOG BEHAVIOR

HDL-A is a VHDL-based analog-behavioral modeling system from Anacad for use with its Eldo simulator. The syntax used in the HDL-A models is based on VHDL syntax, but is extended to allow for the description of complex analog and mixed-signal hardware. It can also describe sampled-data and nonelectrical systems. Consistent with the philosophy of its HDL-D VHDL simulator, Anacad's HDL-A is a compiled-code system that yields high performance. Analog and digital hardware-description code are both compiled to C, and then linked automatically. Two versions of HDL-A are available: one for model execution and one for model development. The software runs on DEC, HP, IBM, and Sun workstations. Pricing for the model-execution and model-development versions is set at $8000 and $30,000, respectively. LM

Anacad Electrical Engineering Software, 4675 Stevens Creek Blvd., Suite 230, Cupertino, CA 95051; (408) 296-8151. **CIRCLE 803**

BOARD DESIGN PACKAGE HAS 32-BIT STRUCTURE

The newest version of the Eagle pc-board design package incorporates an upgrade from a 16-bit to a 32-bit structure. The complete environment consists of schematic capture, board layout, and rip-up autorouting. Other improvements in version 3.0 include copper pouring, forward and backward annotation, 0.01° part rotation, the ability to open several drawings at one time, and Gerber file generation. Users also enjoy extended-memory support, an enhanced library database, and the ability to define 255 layers. Eagle version 3.0 is shipping now. It runs on PCs under DOS or OS/2. The 16-bit Eagle software is still available. Call for pricing information. LM

CadSoft Computer Inc., 801 S. Federal Hwy., Delray Beach, FL 33483; (800) 858-8355 or (407) 274-8355. **CIRCLE 804**

ENHANCEMENTS ADDED TO PC-BOARD DESIGN TOOLS

Pads Software enhanced functions such as cluster placement, via control, and design speed in the latest release of its Pads pc-board design tools. The Pads tools now feature automatic cluster placement, multilayer blind- and buried-via control, and improved graphics performance in the Microsoft Windows environment. The cluster placement option lets users assign components to clusters based on functionality or connectivity. Once this is done, the tool uses a series of automated sweeps to place the clusters, and finally the components themselves. Placement is completely automated, and follows user-defined parameters like standoff and proximity. Another enhancement, increased via control, accounts for board-manufacturing processes. A new form lets users define layer pairs as they will be drilled and plated during the manufacturing process. This prevents the use of vias that cross a pair of layers not drilled and plated together, and helps ensure that the boards that are designed can be built and will work as expected. The Pads pc-board design and layout software runs on personal computers under DOS, Windows, and Windows NT. It also runs on Unix workstations. Call the company for pricing and additional product information. LM

Pads Software Inc., 165 Forest St., Marlboro, MA 01752; (508) 485-4300. **CIRCLE 841**

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HIGH-POWER CONVERTERS SPORT WIDE INPUTS

A wide input range and high efficiency are featured in the 6000 Series of 60-W single-, dual-, and triple-output dc-dc converters. Twenty-four models operate over wide 2:1 input ranges of 9 to 18, 18 to 36, or 36 to 72 V dc. Tightly regulated output combinations include 5, 12, 15, ±5, ±12, or ±15 V dc. Other features include input-to-output isolation of 800 V dc, efficiency as high as 87%, continuous short-circuit protection, output overvoltage protection, and low output ripple and noise. Pricing starts at $104.30 in lots of 100. Delivery is from stock to four weeks. DM

Conversion Devices Inc., 15 Jonathan Dr., Brockton, MA 02401; (508) 559-0880. **CIRCLE 805**

DUAL THYRISTORS CONTROL UP TO 68 KW

Control of ac power to motors, lighting, and temperature-control systems and for solid-state switching applications falls to two families of dual-thyristor and thyristor/diode modules. The MMO types contain two high-voltage thyristors connected in anti-parallel while the MLO modules carry a thyristor connected in anti-parallel with a diode. The MLO/MMO75-12io1 and -16io1 modules are rated at 86 A rms at T_C = 85°C and 1200 and 1600 V, respectively. These units raise the possible power-control level to 68 kW on 460-V, three-phase electrical systems. The MLO/MMO36 modules are rated at 39 A rms and come with either a 1200- or 1600-V rating. In 460-V, three-phase systems, these modules control up to 30 kW. In lots of 100 pricing is $15.28 for the MLO36-12io1, $14.63 for the MMO36-12io1, and $18.53 and $18.95 for the MLO75-12io1 and MMO75-12io1, respectively. Samples are available from stock with larger quantities shipping in six to eight weeks. DM

IXYS Corp., 3540 Bassett St., Santa Clara, CA 95054; (408) 982-0700. **CIRCLE 806**

CONVERTER DELIVERS 5-V-AT-600-MA OUTPUT

The LT1302, an SO-8-packaged dc-dc converter, provides a 5-V output at currents up to 600 mA from a two-cell input with efficiencies up to 87%. Quiescent current for the device is just 200 µA, and that current can be cut to 15 µA by means of a logic-controlled shutdown. High efficiency is maintained over a wide range of output currents by automatic shifting between burst-mode operation at light loads and current-mode operation at heavy loads. An on-chip, low-loss npn power switch handles up to 2 A and can switch at frequencies up to 400 kHz, enabling the use of very small SMT capacitors and inductors. Pricing is $3.21 in an 8-pin DIP and $3.35 in an 8-pin SOIC, both in lots of 1000. Small quantities are available from stock. DM

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 4-LINEAR. **CIRCLE 807**

FRONT-END SUPPLY DRIVES CONVERTERS

The PM33210P, a power-factor-corrected, isolated front-end power supply, provides up to 2100 W in a compact 5-by-5-by-11.5-in. package with hot-swappable Elcon Lower Drawer connectors for powering brick dc-dc converters in distributed-power architectures. The supply features a 48-V, 44-A output as well as wireless programmed droop-current sharing for ease of parallel operation. It also meets IEC 555-2 PFC requirements. Its 3000-V primary-to-secondary isolation enables system integrators to use either isolated or less costly non-isolated distributed converters. Pricing for the PM33210 supply with hot-swap connectors and isolation diodes starts at $990 in single quantity. Delivery is from stock to four weeks. DM

Pioneer Magnetics, 1745 Berkeley St., Santa Monica, CA 90404; Oscar Higgins, (310) 829-6751. **CIRCLE 808**

ULTRA-THIN LITHIUMS POWER PCMCIA CARDS

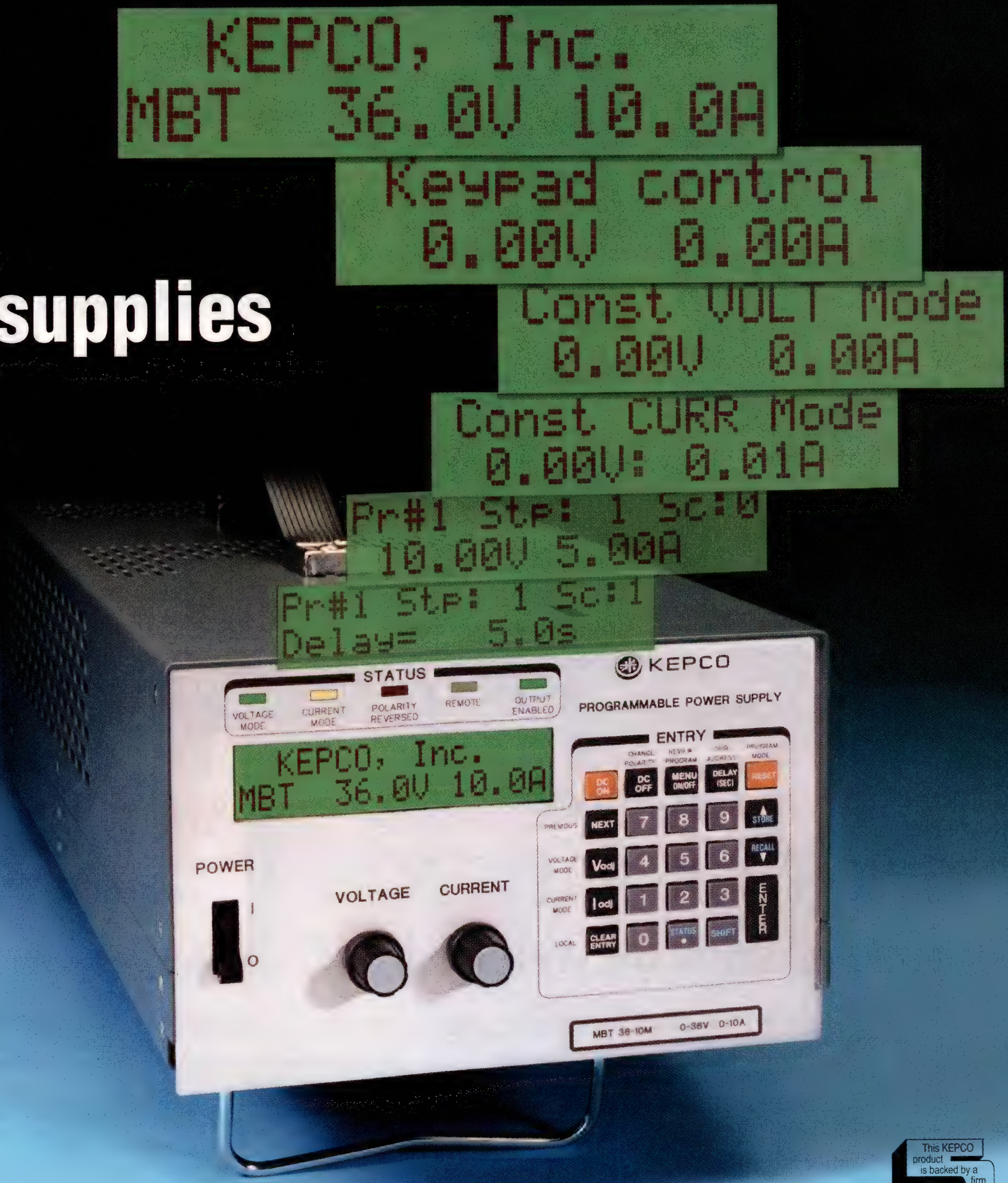
A line of ultra-thin, rectangular POWERDEX lithium primary batteries is available for a wide range of low- and medium-drain applications such as credit cards, super-smart cards, security cards, PCMCIA cards, and lightweight portable systems. The line includes 50-mAh cells as thin as 0.7 mm. They offer high energy density per unit volume and a stable discharge-voltage profile. Copper terminals provide low electrical resistance and wider design flexibility, making it possible to place the cells at the most efficient locations for pc-board routing and product manufacturing. The co-planar copper side-tab configuration permits mounting the cells directly on boards by soldering or spot welding, eliminating the cost and space required for a battery holder. Call for pricing and delivery information. Samples are available for evaluation. DM

Gould Electronics Inc., Electronic Power Sources, 35129 Curtis Blvd., Eastlake, OH 44095-4001; (800) 722-7890. **CIRCLE 809**

SMT POWER MOSFETs BOAST LOW $R_{DS(ON)}$

Compared with previous-generation SMT power MOSFETs, Motorola's high cell density, n- and p-channel and complementary MiniMOS devices feature lower on-resistance—typically 200 mΩ or less. That's because of the company's HDTMOS (high-density TMOS) process that employs VLSI techniques to produce 6 million cells/in.^{2}. The denser cells reduce power dissipation, allow cooler performance, and cut parts counts by eliminating the need to parallel devices. The 12-V parts have a gate-to-source voltage of 2.7 V, making them usable for power management in portables. The MOSFETs are housed in SO-8 (8-pin SOIC) packages whose leadframe realizes maximum thermal transfer. Pricing depends on the specific part, but the MMDF5N03HD goes for $0.89 in OEM lots. Samples are from stock. DM

Motorola Inc., MD Z-311, 5005 E. McDowell Rd., Phoenix, AZ 85018; Scott Delaney, (602) 244-3071. **CIRCLE 810**



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MBT MODEL TABLE

MODEL	OUTPUT VOLTAGE Volts	OUTPUT CURRENT Amperes
MBT 6-32MG	0-6	0-32
MBT 15-20MG	0-15	0-20
MBT 25-14MG	0-25	0-14
MBT 36-10MG	0-36	0-10
MBT 55-7MG	0-55	0-7
MBT 75-5MG	0-75	0-5
MBT 100-3.6MG	0-100	0-3.6
MBT 150-2.4MG	0-150	0-2.4

A single board computer is included in models with suffix "G". This enables the RS 232 & GPIB (IEEE 488.2) ports and allows an MBT to act as a "master" driving other power supplies. Models are available without the G for use as "slave" units and stand-alone service. To include the Output Enable and Polarity Reversal relays, add a suffix "R" to the model number.

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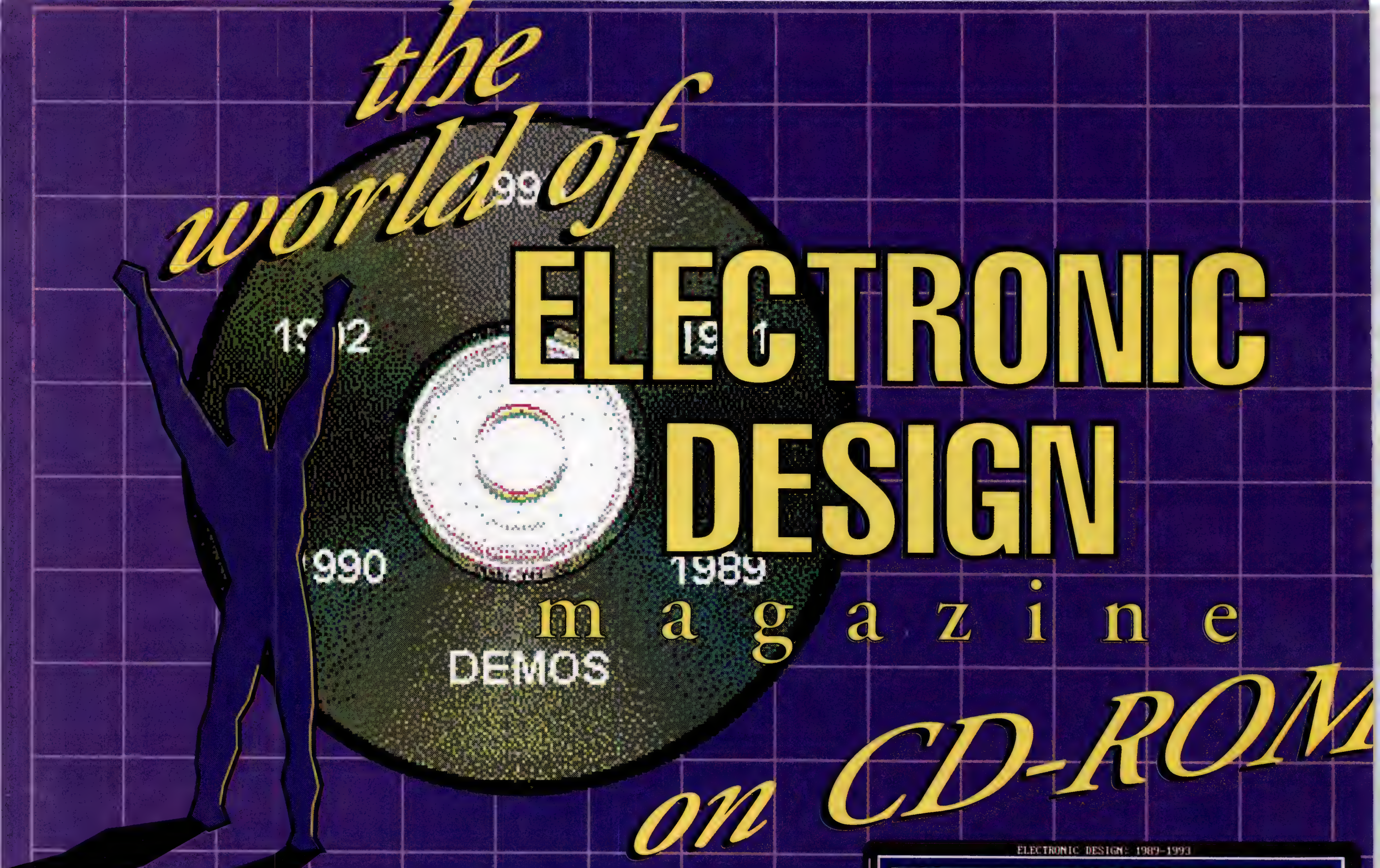

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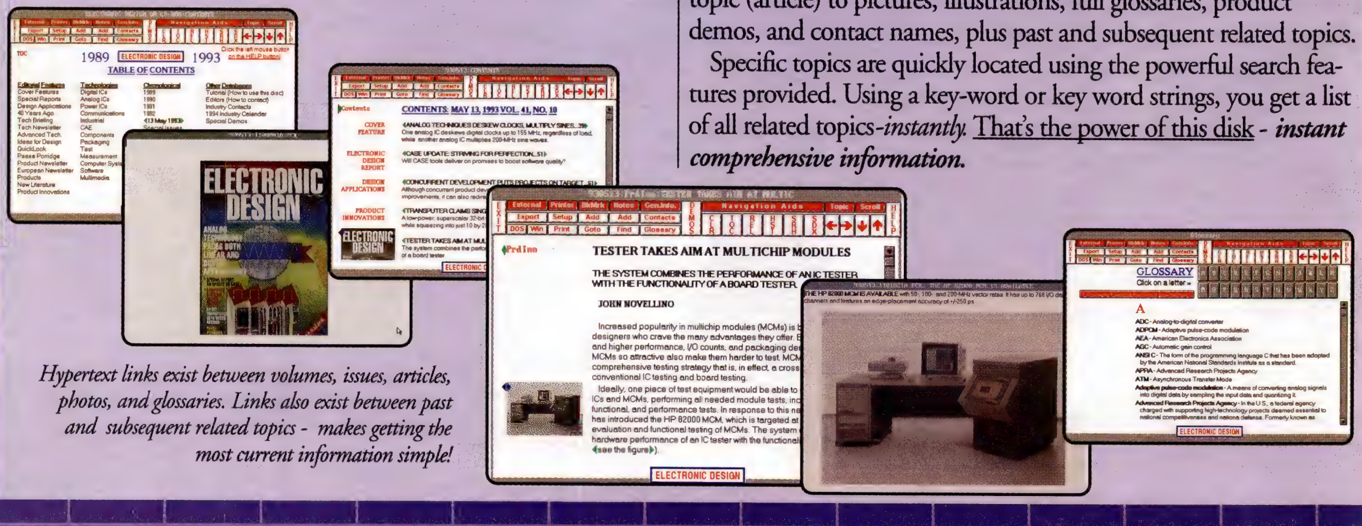

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

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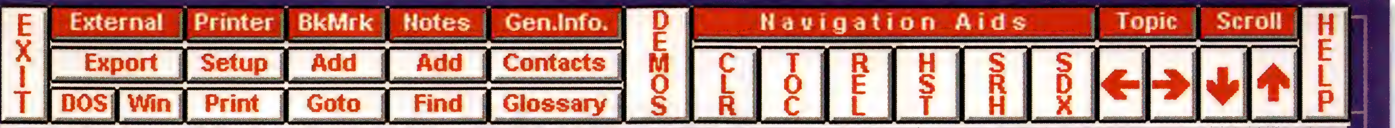

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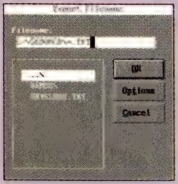

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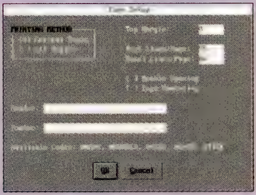
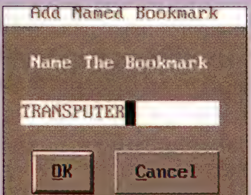
DOS & **Win** - DOS brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. Return to Electronic Design Magazine, where you left off, without re-launching.

Printer Commands

Setup & **Print** - Articles, editorials, glossaries, table of contents, illustrations, and photos (if your printer is capable).



Bookmarks and Notes - *Leaving your mark*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Name The Bookmark

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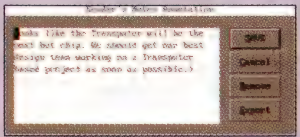
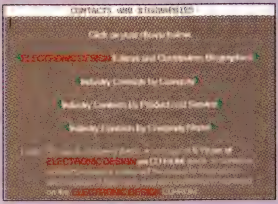
BkMrk - Bookmarks flag topics for future reference, just like using a bookmark in a real magazine. You mark a spot, and the bookmark is stored even if you quit. **GOTO** brings you back to your bookmarks. Deleting them is just as simple.

Notes - Add and find your own notations. Notes stay until you delete them, even after you quit.



Gen. Info - *Complete reference and more!*



Contacts are complete with company and contact names, phone numbers, and addresses. All of the information you'll need to follow up.

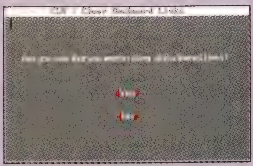
Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

DEMOS - *Instant products demos and information*

This button gives you pertinent product demos and information. Submitted by the manufacturer, demos often include live action footage, most in color.

Navigation Aids - *Magellan you're not, and you don't need to be*

All the aids you'll need to motor your way through this CD in no time flat.

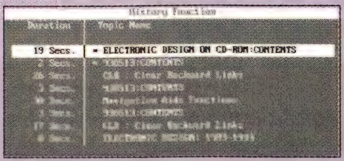


CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.

REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.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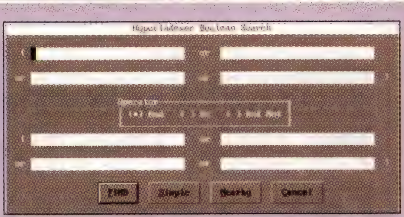

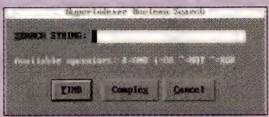

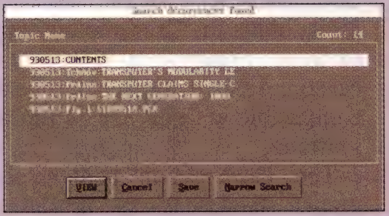
930513:CONTENTS

SRH - *Search* - Conduct simple, complex or proximity indexed searches.

SDX - *Subject Index* - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

Topic Keys - *Issue browsing*

Moves you through an issue article by article, forward or backward.

Scroll Keys - *Leafing through an article*

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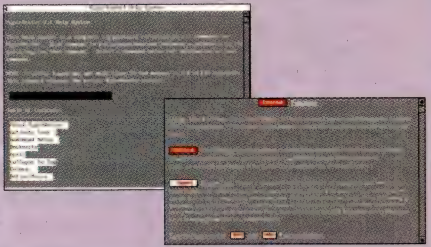

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WORKSTATION HOLDS 125-MHZ PA-RISC PROCESSOR

The high-performance family of HP 9000 Series 700 desktop workstations has a new top-end model—the Model 735/125. The platform, which runs at 125 MHz, holds the first implementation of the company's PA-7150 microprocessor. As a result, it's 100% binary compatible with all Series 700 workstations.

The workstation boasts performance specifications of 136 SPECin92, 201 SPECfp92, 154 MIPS, and 57 MFLOPS. Consequently, it is suited for such applications as electrical and mechanical CAD, electronic design automation, geographic information systems, scientific visualization, and statistical analysis.

Like existing family members, the 735/125 supports a range of integrated graphics-system options, from an eight-plane gray scale to 24-plane accelerated, double-buffered color. Graphics software support includes X11R5, PEX, PHIGS, Starbase, and PowerShade. Maximum configuration includes 400 Mbytes of error-correction system memory and a 2-Gbyte internal hard-disk drive. Using a disk array, storage capacity can be increased to 125 Gbytes. Built-in I/O includes Ethernet, single-ended or fast and wide SCSI-II, and one EISA slot.

The Model 735 is compatible with standard operating systems and user interfaces including HP VUE, OSF/Motif, and the X-Window system. Prices start at $39,995 for an entry-level configuration, which includes a 19-in. color monitor, 32 Mbytes of memory, and a 1-Gbyte hard disk. Systems are available now.

Hewlett-Packard Co., 3000 Hanover St., Palo Alto, CA 94304. CIRCLE 811

■ *RICHARD NASS*

NOTEBOOK WORKSTATION HOLDS POWERPC

Power users can go portable with the RISC System/6000 N40, a PowerPC-based notebook workstation. The platform combines the power of the PowerPC 601 microprocessor with the AIX operating system in a lightweight (6.9-lb.) computer. Running at 50 MHz, the N40 achieves 41.7 SPECint and 51 SPECfp. System memory ranges from 16 to 64 Mbytes, and the internal storage is done on a removable 340-Mbyte drive. The display is a 9.4-in. 256-color active-matrix TFT, which supports resolutions up to 1280 by 1024 pixels. The system is multimedia-ready, with an integrated speaker and microphone. Expansion is handled through two Type II PCMCIA slots. An optional battery pack supplies four hours of operation. RN

IBM Corp., 1133 Westchester Ave., White Plains, NY 10604. CIRCLE 812

MULTIMEDIA KIT OFFERS DRIVE, CARD

Multimedia can be obtained without the hassle of integration—The Vienna Interactive Multi-Media Kit includes a Sony 33A CD-ROM drive and an MV-16 sound card. The drive boats a double-speed transfer rate of 300 kbytes/s and is fully compatible with the MPC-2 specification. It can read CD-DA, CD-ROM XA, CD-1 data, and multi-session photo CD disks. The 16-bit sound card offers ADPCM data compression, four FM operators, and a MIDI interface. Input anti-aliasing and output smoothing filters result in a higher quality sound. RN

Ocean Information System Inc., 688 Arrow Grand Circle, Covina, CA 91722; (800) 325-2496. CIRCLE 813

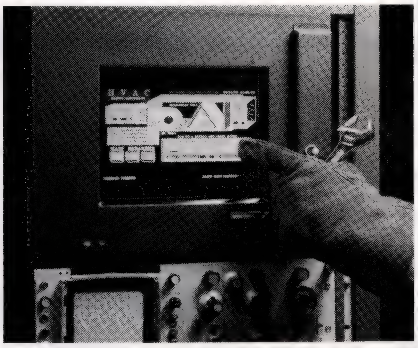
SOUND CARD FITS PCMCIA FORM FACTOR

Users of portable systems can take their audio functionality on the road using the Audio Adapter Card, a 16-bit PCMCIA card. The device adds high-definition stereo sound to most popular applications. It consists of a Type II card that's connected to a small detachable tethered Audio Interface Module (AIM). The AIM module features a built-in mono microphone, a stereo line-in input (an external microphone input), and a stereo output (headphone) jack. The integrated 16-bit CODEC permits playback and record of up to 48,000 samples/s using 8- or 16-bit resolutions in stereo or mono form. Drivers are included for DOS, Windows, and OS/2. The audio card will enable such popual applications as IBM StoryBoard, Microsoft Video for Windows, Lotus Freelance Graphics, and WordPerfect Presentation. In quantities of 1000, the Audio Adapter Card is priced at $150 and is available for immediate delivery. RN

IBM Microelectronics, 1580 Route 52, Internal Zip B, Hopewell Junction, NY 12533; (800) IBM-0181. CIRCLE 814

INDUSTRIAL COMPUTER HOLDS 486DX

Designed for harsh environments, the SealTouch industrial computer is built with a 33- or 66-MHz 486DX microprocessor. The rugged platform contains an infrared touch system and is housed in a panel-mount configuration that can be integrated into a custom enclosure. It also features a sealed active-matrix 10.4-in. color VGA display, an internal 3.5-in. floppy-disk drive, a 120-Mbyte hard-disk drive, and four full-size expansion-card slots.

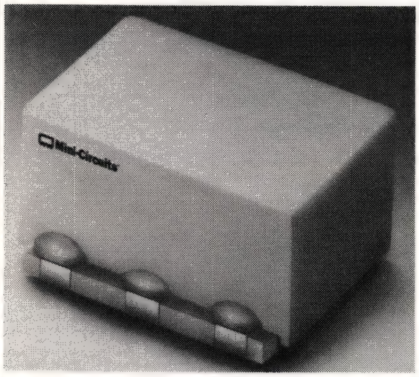


The system measures 12.3 by 15.5 by 7.06 in. and weighs 15.5 lbs. Display options include either an active-matrix color TFT LCD or an EL gray-scale unit. DOS comes bundled with the platform. Prices for the SealTouch computers run from $9565 for the 33-MHz model to $12,685 for a 66-MHz unit. RN

Deeco Systems, 31047 Genstar Rd., Hayward, CA 94544; (510) 471-4700. CIRCLE 815

MINIATURE MIXER COVERS 5 TO 1900 MHZ

Measuring just 0.25 by 0.31 by 0.2 in., the RMS-11X surface-mount mixer serves high-volume cellular and PCN applications in the range of 5 to 1900 MHz. The all-ceramic unit has a 1-dB compression at a 1-dBm RF input with 6-db conversion loss and specs that are statistically controlled to better than 4.5 σ from mean. All connection pads have solder over nickel barrier for improved leach resistance and excellent solderability. Other features include all-welded internal construction that'll pass MIL-M-28837 shock and vibration tests. Pricing is $3.95 in quantities of 10 to 49. Units are available on tape-and-reel. DM

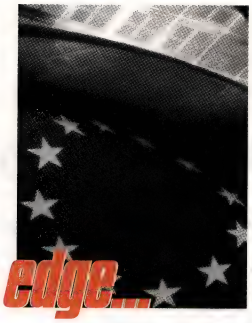


Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235-0003; (718) 934-4500. **CIRCLE 816**

TELECOM TRANSFORMERS MOUNT IN THROUGH HOLES

Designed for high-speed data applications, the SPT-022 and SPT-023 through-hole-mount telecommunication transformers match 600-Ω primary and secondary impedances at zero dc loop currents. Total harmonic distortion for both units is –76 dB typical for the -022 and –82 dB typical for the -023 (measured at –10 dBm, 600 Hz). This makes both transformers suitable for high-speed V.32bis applications. Both are designed for FCC/DOC applications. Overall dimensions for both are 1.024 in maximum length by 0.945 in. maximum width by 0.472 in. maximum height. Pricing in lots of 5000 is $2.15 for the SPT-022 and $2.79 for the SPT-023. Delivery is from stock. DM

Prem Magnetics Inc., 3521 N. Chapel Hill Rd., McHenry, IL 60050; (815) 385-2700. **CIRCLE 817**



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The Portable By Design Conference and Exposition

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Electronic Design is soliciting technical papers to be presented at the Portable By Design Conference February 15-17,1995 in the Santa Clara Convention Center, Santa Clara, Calif.

Engineers experience in designing portable electronic systems of all types are invited to share their expertise. The range of eligible design applications includes computing, communications, data-entry, navigation and instrumentation-in either vertical and horizontal markets.

Papers should emphasize problem solving and provide insights into specifying and designing portable systems.

General topics to be covered include: Microprocessors and microcontrollers;Power Sources and circuits;Power management techniques; Batteries; Connectivity(e.g. docking, public wired network and all wireless); Software(e.g. operating systems including proprietary OS and application development); Peripherals (e.g. PCMCIA, GPS, storage); Displays; Input devices; and, System design considerations (e.g. accelerated product development, testing, size, ergonomics and ruggedness)

To participate, respond to this call for papers by sending a one-paragraph abstract of a paper you would like to present. Papers should be oriented toward solving specific design problems.

Abstracts should be sent to: *Program Chair, Portable By Design* Conference, c/o Electronic Design Magazine, P.O. Box 821, Hasbrouck Heights, NJ 07604. Or, send by fax to (201) 393-0204.

Deadlines:

Abstracts: October 10,1994

Full Papers: December 1,1994

FLAT-PLASMA DISPLAY FOR HDS APPLICATIONS

The 1024-768 SVGA Video Display, developed for high-definition-system (HDS) applications, offers luminosity, chromaticity, and uniformity approaching the performance of CRTs. It comes in a 30-package that's thin enough to be hung on the wall like a picture. Developed using the company's Double Substrate High Resolution Barrier (DSHRB) alternating-current color plasma display (AC-PDP) technology, it currently holds the record for the highest picture resolution (1024 by 768 full-color pixels) for large-area flat-panel displays.

The double-substrate high (two electrode) resolution AC-PDP structure is the key to the 1024-768 display, providing for full-color performance and excellent memory margin with high brightness. The display offers 43 pixels/in. resolution, with 64 (6-bit) gray levels, and a 60-fps progressive scan. With a black-matrix-type pixel structure, the area contrast ratio for white pixels is greater than 100:1. In addition, the display has a wide viewing angle of greater than 160°. It comes complete with a color panel, drive electronics, power supply, and standard, analog RGB (SuperVGA), video interface.

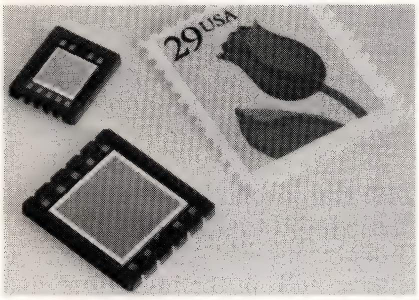
Depending on the application of this display, it can be easily manufactured to meet the environmental, reliability, and quality requirements for industrial and military purposes. Prototype demonstrations of the units are currently being arranged. The full-color, alternating-current-plasma display will be available for engineering evaluation in the first quarter of 1995.

Photonics Imaging, 6975 Wales Rd., Northwood, Ohio 43619; Beverly Denny, (419) 666-6325. CIRCLE 818

■ *CHERYL AJLUNI*

P-I-N PHOTODIODE IS SURFACE-MOUNTABLE

Applications in laser radar detectors, bar-code readers, and consumer products are possible for the S5106 and S5107 surface-mount, chip-carrier-type silicon p-i-n photodiodes. The devices have large active areas, which allow detection with a wide angle of acceptance. Their chip-carrier packages are suitable for surface mounting and are just 1.26 mm thick. Sensitivity is 0.72 A/W at 960 nm. Reverse voltage is 30 V, power dissipation is 50 mW, and operating temperatures range from –20 to 60°C. Dark current is typically 0.3 nA for the S5106 and 1 nA for the S5107. Both devices are from stock. DM



Hamamatsu Corp., 360 Foothill Rd., Box 6910, Bridgewater, NJ 08807-0910; (908) 231-0960. CIRCLE 819

LOW $R_{DS(ON)}$ MOSFETS COME IN SMT PACKAGES

A high-current, low on-resistance n-channel MOSFET is claimed to offer the lowest on-resistance available in TO-92 and SOT-89 packages. The VN3205 is rated at BV_{DSS} = 50 V minimum and has a maximum gate-source threshold voltage of 2.4 V. The maximum on-resistance is 0.3 Ω at V_{GS} = 10 V and it is 0.45 Ω at V_{GS} = 4.5 V. In addition to the SMT SOT-89 and TO-92 packages, it's also offered in 14-pin quad plastic DIPs and in die form. The 2.4-V threshold voltage ensures compatibility with TTL and 3-V logic circuits. Applications include medical equipment, telecommunication, motor controls, instrumentation, and battery-operated systems. Pricing for the VN3205N8 (SOT-89) is $0.56 in lots of 1000. Samples are delivered from stock and lead time for production lots is four to six weeks. DM

Supertex Inc., 1350 Bordeaux Dr., Sunnyvale, CA 94089; Dilip Kapur, (408) 744-0100. CIRCLE 820

SMT ZENER DIODES BOOST DESIGN DENSITY

Greater board density and design efficiency is available to users of the RSZ5200 Series surface-mounted Zener diodes. The 1N5200-compatible diodes are housed in SOT-23 packages and are available from 2.4 to 51 V. Power dissipation is 225 mW. Features include a silicon planar construction with an operating-temperature range of –55 to +150°C. The diodes are a useful source of voltage regulation for automotive, telecommunication, and computer application where size and density requirements are critical. They're packaged in 8-mm plastic carrier tape in quantities of 3000 (7-in. reel) and 10,000 (13-in. reel). Pricing is under $0.04 in million-piece lots. Delivery is in 14 weeks. DM

ROHM Corp., 3034 Owen Dr., Antioch, TN 37013; Lee Burgess, (615) 641-2020, ext. 134. CIRCLE 821

MOVS SUPPRESS DAMAGING TRANSIENTS

Four metal-oxide varistors (MOVs) in 14- and 20-mm packages extend the operating voltage and energy ratings of Harris's C-Series III MOV family. The new family members provide continuous rms operating voltages of 230, 250, 275, and 300 V and energy ratings to 240 J. Optimized for surge suppression in power-supply and motor-control applications, as well as transient-voltage surge-suppression modules, the devices shunt currents of 6000 A (14-mm types) and 9000 A (20-mm types). UL Standard 1449 specifies maximum surge-transient withstand capabilities, calling for protection devices to weather three worst-case pulses. The 20-mm devices are conservatively rated for 20 such pulses, while the 14-mm units are rated for 10, which is also conservative. Pricing is $0.60 for the 14-mm units and $0.70 for the 20-mm types, both in lots of 10,000. Delivery is from stock. DM

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; (800) 4-HARRIS, ext. 7205. CIRCLE 822

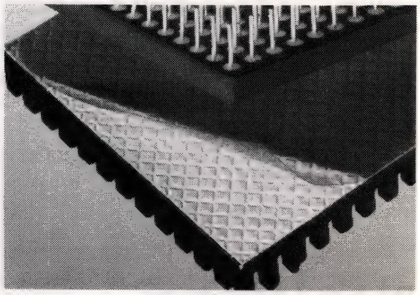
RESIN SYSTEM REPLACES FR-4

For its standard process regimen, QLP Laminates has adopted a Multi-Plus blended-epoxy resin system, displacing FR-4 for mass-laminate and multilayer boards. The Multi-Plus pre-preg and multilayer laminates boast a nominal T_g of 145°C. They're well suited for manufacturing high-reliability multilayer packaging because they withstand repeated exposure to soldering temperatures and harsh chemical cleaning processes without measeling, crazing, or delaminating. A data sheet is available free of charge. Call for information. DM

QLP Laminates Inc., 4955 E. Hunter Ave., Anaheim, CA 92807; (714) 970-1471. **CIRCLE 823**

THERMAL TAPES BOND DEVICES TO HEAT SINKS

Tight bonds between heat sinks and hot-running components without mechanical fasteners or liquid adhesives are achieved using Thermattach T412 thermally conductive, double-sided adhesive tape. The tape



features exceptional thermal conductivity of 1.4 W/m-K and a thermal impedance of only 0.25°C-in.^{2}/W. It offers an embossed surface that enhances both conformability and thermal performance. Tapes are available in standard roll widths, and pre-cut parts come in kiss-cut, rectangular shapes on rolls. Call for pricing and delivery. DM

Chomerics Inc., 77 Dragon Ct., Woburn, MA 01888; (617) 935-4850. **CIRCLE 824**

220-MM ETSI RACK MANAGES CABLING

Outstanding cable-management facilities, both in the rack itself and through a range of dedicated accessories, is provided by the 220-mm-high ETSI rack. Available in both 600-by-300- and 600-by-600-mm plan sizes, the rack fully conforms to the latest European Telecommunications Standards Institute (ETSI) draft. It accepts both 450- and 500-mm-wide subracks, and adapter-panel mountings are available to allow mixed 19-in. and hard-metric technology. Made from pre-galvanized steel, the rack comes configured to user requirements. Pricing is around $450 and varies with configuration. Delivery is in from two to four weeks. DM

BICC-VERO Electronics Inc., 1000 Sherman Ave., Hamden, CT 06514-1336; (800) 242-2863. **CIRCLE 825**

FROM CONCEPT TO ARTWORK IN 1 DAY

ULTIboard, one of the leading PC based design systems, is supplied worldwide via a network of ULTImate Technology offices and distributors. ULTIboard's success in the professional design community is primarily due to its superior interactive functionality.

Real Time Placement Aids, Real Time Design Rule Check, Trace Reroute While Move and Trace Shove, are all features wich will dramatically reduce your design time.

Integration with ULTIcap guarantees smooth data flow between Schematic and PCB editing and the inclusion of third party netlist interfaces ensures ULTIboard will fit into any design environment.

Another of ULTImate Technology's strengths is our flexible growth path. Users may start with a low cost ULTIboard Challenger Lite and grow, step by step, to a 32-bit Advanced system with Ripup and Retry Autorouting.

ULTImate Technology also looks after existing users, providing they have valid mainenance subscriptions they will be upgraded to a new system based on their original investment. For instance, a 1987 ULTIboard-DOSsystem has now been up- graded to a 32-bit Advanced system with Windows compliance and 2 Autorouters.

ULTImate Technology not only adds value to your investment in an ULTIboard system but backs it up with the highest quality support from our distributors and offices.

ULTIBOARD
= PRODUCTIVITY
The European quality alternative

More than 10.000 Users

Your design ideas are quickly captured using the ULTIcap schematic design Tool. ULTIcap uses REAL-TIME checks to prevent logic errors. Schematic editing is painless, simply click your start and end points and ULTIcap automatically wires them for you. ULTIcap's auto snap to pin and auto junction features ensure your netlist is complete, thereby relieving you of tedious netlist checking.

ULTIshell, the integrated user interface, makes sure all your design information is transferred correctly from ULTIcap to ULTIboard. Good manual placement tools are vital to the progress of your design, therefore ULTIboard gives you a powerful suite of REAL-TIME functions such as, FORCE VECTORS, RATS NEST RECONNECT and DENSITY HISTOGRAMS. Pin and gate swapping allows you to further optimise your layout.

Now you can quickly route your critical tracks. ULTIboard's REAL-TIME DESIGN RULE CHECK will not allow you to make illegal connections or violate your design rules. ULTIboard's powerful TRACE SHOVE, and REROUTE-WHILE-MOVE algorithms guarantee that any manual track editing is flawless. Blind and buried vias and surface mount designs are fully supported.

If you need partial ground planes, then with the Dos extended board systems you can automatically create copper polygons simply by drawing the outline. The polygon is then filled with copper of the desired net, all correct pins are connected to the polygon with thermal relief connections and user defined gaps are respected around all other pads and tracks.

ULTIboard's autorouter allows you to control which parts of your board are autorouted, either selected nets, or a component, or a window of the board, or the whole board. ULTIboard's intelligent router uses copper sharing techniques to minimise route lengths. Automatic via minimisation reduces the number of vias to decrease production costs. The autorouter will handle up to 32 layers, as well as single sided routing.

ULTIboard's backannotation automatically updates your ULTIcap schematic with any pin and gate swaps or component renumbering. Finally, your design is post processed to generate pen / photo plots, dot matrix/ laser or postscript prints and custom drill files.

SPECIAL OFFER

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- 100% compatible with higher capacity versions without loss of investment

Also available is a full function (as described above, with a 150 pin design capacity)Evaluation System for only US$ 40 excl shipping/handling, VAT/Sales Tax).

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READER SERVICE 137

TOOL MANAGES DSP CODE DEVELOPMENT

SwiftNet 2.1, a bidirectional communications protocol for developing code for embedded DSP applications, manages the connection between Pentek software development tools running on popular workstations and its VMEbus DSP products based on TI C30 and C40 DSP processors. SwiftNet handles multiprocessor boards and target devices by maintaining a network directory of all DSP target devices for single VMEbus card cages and distributed systems of multiple card cages. A VxWorks Developer's SwiftNet API (Model 4941) for 68030 and 68040 boards supports Ethernet connection to Sun workstations. A runtime EPROM version of SwiftNet (Model 4940) turns the CPU board into an Ethernet-to-VME adapter. Contact the company for pricing. SVT

Pentek Inc., 55 Walnut St., Norwood, NJ 07648; (201) 767-7100; fax -3994. **CIRCLE 826**

PROJECT MANAGEMENT TOOL AIMS FOR UNIX

AutoPlan II Version 2.0 project-management software for Unix includes the InterProject Bulletin Board and the AutoPlan Programming Interface (APPI). The new version increases the ability of AutoPlan II to automatically access and integrate data from other projects and geographical distances with up-to-the-minute accuracy. The bulletin board creates an information network between projects and people in the work group. Messages are viewed in the project's bulletin board, giving members up-to-date information. A calendar pool stores data for individuals and projects. Annotation capabilities enable users to write text notes attached to or pointed at tasks in graphical reports. Pricing for Autoplan II starts at $1495. SVT

Digital Tools, 18900 Stevens Creek Blvd., Cupertino, CA 95014; (408) 366-6920; fax (408) 446-2140. **CIRCLE 827**

ADD SERIAL I/O TO PC PROGRAMS

The Software Wedge adds two-way serial I/O capabilities to DOS, Windows, OS/2, or NT applications. The software links with PC-based electronic scales, lab instruments, bar-code readers, and other data collection instructions. Professional versions include the ability to parse and filter incoming data and to add keystrokes or date/time stamps. Other features include timed automatic output strings, hot-key activated output strings, input data translation tables, and support for 16550 UARTs. DOS and Windows versions have serial diagnostic utilities for debugging communications. Professional DOS edition is $295; a Windows version is $395. Standard edition is $199 for Windows, $129 for DOS. SVT

T.A.L. Enterprises, 2022 Wallace St., Philadelphia, PA 19130; (215) 763-2620 or (800) 722-6004. **CIRCLE 828**

Interactive Analog Simulation

ICAP/4, The Virtual Circuit Design Lab, is a complete circuit design system featuring schematic entry, interactive analog and mixed signal simulator, extensive device libraries, and powerful data processing, all integrated in one easy to use environment. With ICAP/4 you can simulate all types of designs include Power, ASIC, RF, Mixed Mode, Control Systems, and Mixed Technologies.

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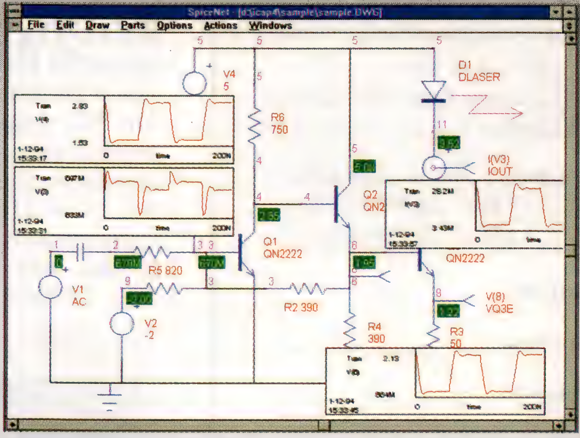

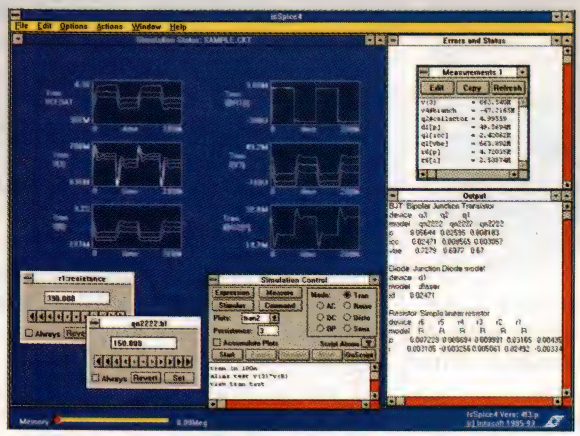

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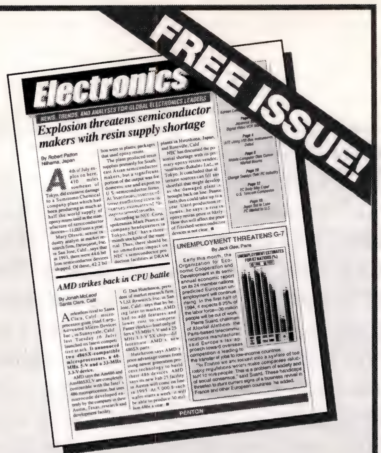

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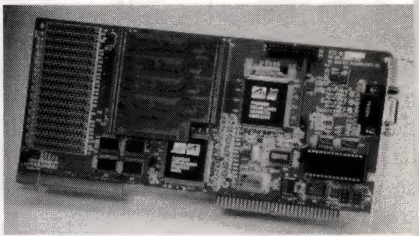
64-BIT ACCELERATOR BETTERS 100 WINMARKS

With a performance specification of over 100 million Winmarks, the 64-bit Graphics Pro Turbo accelerator board is built with the ATI mach64 graphics chip. Aimed at professional true-color graphics applications, including computer-aided design and desktop publishing, the board is available in two memory configurations—either 2 or 4 Mbytes. As a result, it can handle resolutions up to 1280 by 1024 pixels, non-interlaced. The 2-Mbyte model is the base configuration, and the second 2 Mbytes of memory is added through a daughtercard.

Extensive software utilities are bundled with the Graphics Pro Turbo. A DeskTop control panel offers easy access to frequently used graphics-card functions. The FlexDesk control panel supplies quick access to the WinSwitch utility, which permits on-the-fly Windows mode selection, without restarting Windows. The Display Power Management Signaling (DPMS) function shuts down the monitor to reduce the power consumption.



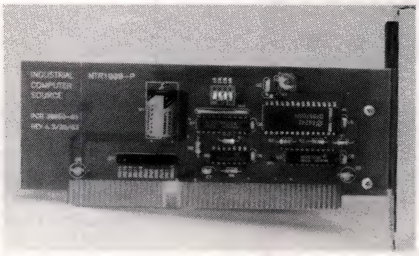
Drivers are available for Windows, Windows NT, and OS/2. There are also specialized drivers for popular applications, including AutoCAD, Microstation, and CADKey. The board can connect to the ISA bus, the VL-Bus, or the PCI local bus. The 2-Mbyte board is priced at $599, while the 4-Mbyte model sells for $899. The 2-Mbyte upgrade module costs $399. All versions are available now.

***ATI Technologies,** 33 Commerce Valley Dr. E., Thornhill, Ontario, Canada L3T 7N6; (905) 882-2600.* **CIRCLE 829**

■ *RICHARD NASS*

REAL-TIME CLOCK BOASTS HIGH ACCURACY

The NTR1000-P real-time clock card for PCs supplies a stability of ±5 seconds per month in harsh operating environments, ranging from 0 to 50°C. Suited for control and test-and-measurement applications, the card is built with National Semiconductor's DP8570A clock with battery back-up, and is referenced to a stable crystal with a known aging rate. A Novell driver is included. The NTR1000-P costs $199. RN



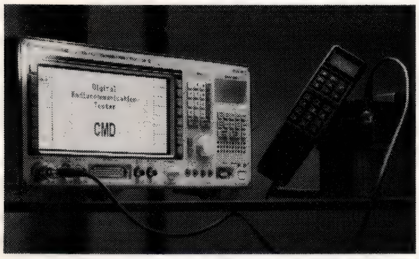
Industrial Computer Source, 10180 Scripps Ranch Blvd., San Diego, CA 92131; (800) 523-2320. **CIRCLE 830**

ACCELERATOR BOARD OFFERS VISUAL REALISM

A Windows accelerator brings a high level of visual realism to mainstream PCs using resolutions of 1024 by 768 pixels. The Pro Graphics 1024 speeds the processing of graphics, text, and video, while supporting 16.7-million colors. Three versions are available—for the VL Bus, the ISA bus, and PCI. For applications that require motion video, the board's hardware feature, FastFilm, accelerates AVI playback for fast, smooth digital-video replay. Standard AVI files can be enlarged to fill the whole screen and played back at up to 30 frames/s without any jerky movements. On-board connectors allow for future upgrades. Most popular DOS applications are supported. Display drivers for OS/2 and Windows NT will be available shortly. Prices start at $395. RN

Media Vision Inc., 47300 Bayside Pkwy., Fremont, CA 94538; (510) 770-8600. **CIRCLE 831**

GSM TEST SET PERFORMS PASS/FAIL OR ANALYSIS



The CMD 52 digital radiotelephone test set is optimized for both pass/fail testing and detailed analysis of global system for mobile communication (GSM) transceivers. The tester incorporates an rf signal generator covering the 935.2-to-959.8-MHz GSM band, a peak-power meter that covers 800 to 1000 MHz and measures output power from 10 to 47 dBm, a dc voltmeter, a current-averaging dc ammeter, and extensive signaling capabilitites. Measurements also include fast power ramping, phase and frequency error, and bit error rate with the addition of the CMD-B4 add-in card. Major test functions include mobile synchronization; location update; incoming and outgoing call setup; peak and power-level control; channel change; received signal level, quality, and strength; echo; call clearing; and dc voltage and current. Softkey controls, intuitive internal software, and a large, high-resolution, backlit LCD display make the instrument easy to use. The CMD 52 costs $23,310, with delivery in 14 weeks. JN

Tektronix Inc., Test & Measurement Group, P. O Box 1520, Pittsfield, MA 01202; (800) 426-2200. **CIRCLE 832**

MODULES, CHASSIS BOOST EMBEDDED COMPUTERS

A flat-panel controller, four I/O modules, and two chassis create a major expansion of the Embedded Modular Computer (EMC) line. The five EXM series cards are designed to fit in the small and rugged EMC systems and are also compatible with the company's VME and VXI families of embedded PCs. The EXM-23 LCD controller supports monochrome and gray-scale LCD and EL displays, and color LCD/TFT displays. The module costs $247 (all prices are for quantities of 50). The EXM-19 is a 24-line optoisolated digital I/O module priced at $179. The EXM-24 is an intelligent eight-port serial RS-232 communications module compatible with the Digiboard PC/8i. It costs $828. The EXM-28 is an Arcnet networking module priced at $208. The EXM-29 is a Fastcomm/422-compatible dual-port RS-422/485 serial communication module costing $200. One new chassis is the EMC-CH10D, which holds 10 EXM cards and connects to a floppy disk module and power supply. It costs $213. The EMC-CH6AT chassis holds six EXM cards and connects to a power supply and standard PC/AT slot. The ECM-CH6AT and a 50-W ac supply cost $950. JN

RadiSys Corp., 15025 S.W. Koll Pkwy., Beaverton, OR 97006-6056; (503) 646-1800. **CIRCLE 833**

EMULATOR RUNS 80C186, 8086/8 TO 30 MHZ

The ET-iC186 supplies full-speed emulation up to 30 MHz for the 80C186/8, and 8086/8 microprocessor families. The real-time emulator operates without wait states or intrusion on I/O or interrupt pins. The clock source is switchable between the target system and the on-board programmable oscillator. The instrument comes with a standard user interface and Paradigm's Debug and Locate development tools. The source-level debugger screen displays either C source code, the corresponding assembly code, or both. The user interface, which includes pull-down menus, mouse support, and context-sensitive on-line help, makes it easy to integrate third-party C compilers, assemblers, and linkers. The system can be configured with 1 Mbyte of zero-wait-state overlay RAM, 1 Mbreakpoints, and a trace option. The real-time trace buffer can record 8 kframes with external triggers, and the trace display shows the source, assembler, and bus cycles. The ET-iC186 starts at $3600. Adapters for emulator-pod-to-target-board connections start at $350. The trace option costs $720. Delivery is in 10 days. JN

Emulation Technology Inc., 2344 Walsh Ave., Bldg. F., Santa Clara, CA 95051-1301; (408) 982-0660. **CIRCLE 834**

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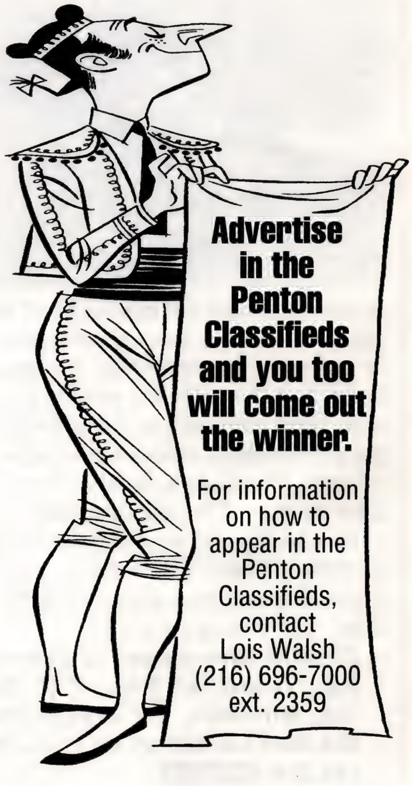
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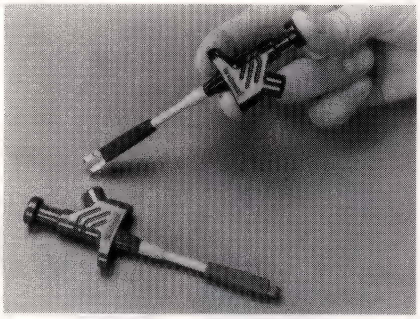
1-GHZ SWITCHING MODULE WORKS WITH ARINC 608A

The 1277-540 Series switching modules allow users to switch signals up to 1 GHz through the Arinc 608A interface. The switch is configured as nine 1-by-4 tree multiplexers and up to six RF splitters. At 100 MHz, insertion loss is less than 0.5 dB; crosstalk is less than –95 dB; isolation is less than –80 dB; and VSWR is 1.2:1. Maximum switchable voltage is 30 V dc. Switchable current is 1.5 A per channel, and switchable power is 60 W dc, 60 VA, or 60 W of RF. The three versions include the 1277-540A with no RF splitters, the 1277-540B with three splitters, and the 1277-540C with six splitters. The units work with the 1277 Arinc 608A mainframe and interface or the 1262-77 VXI mainframe with an Arinc 608A subchassis. Prices start at $5775, with delivery in 10 to 12 weeks. JN

Racal Instruments, 4 Goodyear St., Irvine, CA 92718; (800) 722-3262 CIRCLE 835

WIDE-JAW TEST PROBE HANDLES UP TO 1000 V

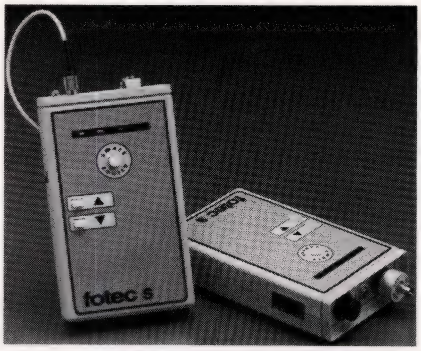
The KLEPS 280 test probe features a steel, spring-loaded, clamp-style jaw that opens to a wide 0.86 in. (22 mm) to accommodate a large range of test connections. The jaws simultaneously open and extend from the probe body, and then close to ensure a reliable, tight connection. A molded handle with socket accepts 4-mm banana plugs with either a fixed or retractable sleeve. The combination provides shock-proof connections for up to 1000 V. The KLEPS 280 costs $19 in small quantities. Delivery is from stock to six weeks. JN



Richard Hirschmann of America Inc., Industrial Row, P. O. Box 229, Riverdale, NJ 07457; (800) 225-0524 ext. 230 or (201) 835-5002 ext. 230 CIRCLE 836

FIBER-OPTIC SOURCES SIMPLIFY TESTING

A series of fiber-optic test sources, called SmartSources, simplifies the testing of fiber-optic cables and other components. When used with an FM300-series fiber-optic power meter, SmartSources synchronizes all meter and source functions for loss testing and outputs the results to a printer or PC. In conjunction with the FOtest software, the instruments perform standard tests automatically, graphically showing the user how to run the test. The SmartSources, FM300 power meters, and FOtest software run on desktop or portable computers for use in the laboratory or in the field. SmartSources come in versions to match all types of fiber-optic systems, with prices starting at $1350. JN



Fotec Inc., 529 Main St., Boston, MA 02129; (800) 537-8254 or (617) 241-7810. CIRCLE 837

MICROWAVE GENERATORS HANDLE MULTIPLE TASKS

The 68000B synthesized CW generators and 68100B synthesized sweep generators are designed to offer the features, performance, and price levels needed for local oscillator substitution, network analysis, and ATE applications. The 68000B supplies precise CW and digitally stepped signals for LO substitution and stimulus tasks. The 68100B adds sweep capability and external am, fm, and square-wave modulation for network analysis. Both have 1-kHz frequency resolution (0.1-Hz optional), less than 80 dBc/Hz ssb phase noise at a 10-kHz offset from 10 GHz, wide dynamic range, and less than 25-ms switching times. Spurious emissions are –60 dBc, and the instruments are IEEE-488 programmable. Both series are available in six models covering frequencies up to 40 GHz. Prices start at $20,500, with delivery in four weeks. JN

Anritsu Wiltron Sales Co., 685 Jarvis Dr., Morgan Hill, CA 95037-2809; (408) 776-8300. CIRCLE 838

100-KHZ, 12-BIT DATA BOARD USES ONLY 1.5 W

A 100-kHz, 12-bit board has been added to the PCI-20377W series of low-power, multifunction data-acquisition boards. Combined with its short length, the PCI-20377W-2's power consumption of only 1.5 W makes it ideal for remote and portable applications. Features include 16 single-ended or eight differential analog inputs; programmable gains of 1, 10, 100, and 200; eight digital inputs; eight digital outputs; a rate generator; two 16-bit counters; DMA support; a sequential channel scanner; built-in zero reference; a 16-word FIFO buffer; and separate digital and analog connectors for reduced noise. Inputs can range from 0 to 10 V to ±0.025 V full scale. The configuration is fully software controlled. The PCI-20377W-2 is available immediately for $525. JN

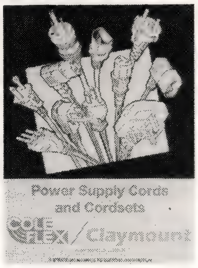
Intelligent Instrumentation, 6550 S. Bay Colony Dr., MS 130, Tucson, AZ 85706; (800) 685-9911 or (602) 573-0887. CIRCLE 839

30-MHZ SCOPE OFFERS 2 MV/DIV. SENSITIVITY

The HM303 is a dual-channel 30-MHz oscilloscope with a sensitivity of 2 mV/div. and a broadband design that limits overshoot to 1%. A built-in dual-frequency (1 kHz/1 MHz) calibrator allows users to perform probe-compensation adjustments in order to optimize fidelity. The fastest sweep rate is 10 ns/div., using the times 10 magnifier. The HM303 can trigger on signals greater than 100 MHz and on inputs of less than one-half a division. An active sync-separator permits detailed examination of TV signals. A built-in component tester uses a stabilized measurement voltage to test active and passive components with a button push. The HM303 costs $548. JN

Hameg Instruments, 1939 Avenida Plaza Real, Oceanside, CA 92056; (800) 247-1241 or (619) 630-4080. CIRCLE 840

CORDS AND CORDSETS FEED POWER SUPPLIES



Detachable and non-detachable power cords and cordsets, jumper cables, and special designs are described in the eight-page Catalog PSC-94 from Cole-Flex, West Babylon, N.Y. Many products carry UL and CSA acceptance as well as numerous international approvals. Cords and cordsets are suited for use in consumer and industrial devices such as tools, appliances, process controls, business machines, computers, communication equipment, and hospital-grade or medical-instrumentation applications. The catalog includes technical information, standards, selection guides, cross references, and an OEM design FAX form for requesting quotes on custom designs. DM **CIRCLE 940**

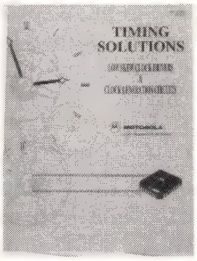
BREAKERS AND RELAYS WITHSTAND HEAVY DUTY

Circuit breakers and relays rated for high-volume appliance and HVAC applications are detailed in the 32-page Catalog 13C220 from Potter and Brumfield Inc., Princeton, Ind. Information is included on thermal circuit breakers as well as both pc-board and panel-mount relays. Circuit breakers offer ratings from 0.5 through 20 A in rocker-actuated and push-to-reset types. Relays are offered with maximum contact ratings from 1 to 30 A. Both open-frame and enclosed models are described. A selector-guide section helps readers quickly determine which product series is best for a given application. DM **CIRCLE 941**

GUIDE DETAILS NO-CLEAN SOLDER PASTES

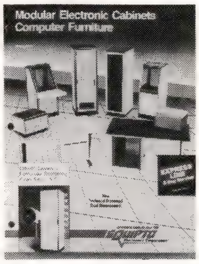
An illustrated 12-page primer from Heraeus Inc., Cermalloy Div., West Conshohocken, Pa., explains how to evaluate, select, and wring the best performance from no-clean solder pastes. The guide provides generic, detailed information to all pc-board assemblers who must cease using solder pastes that require cleaning with CFC-bearing solvents. Clear, concise text explains what a no-clean paste is and whether or not it can be used as a drop-in replacement for solvent-based cleaning. Recommendations cover what to look for when evaluating pastes and discusses reflow profiles. DM **CIRCLE 942**

DATABOOK ADDRESSES CLOCK DISTRIBUTION



Designers of clock-distribution circuits will find a great deal of useful information in the 190-page Timing Solutions data book from Motorola, Phoenix, Ariz. Catalog BR1333/D spans the industry's broadest offering of timing circuits for all logic technologies including TTL, CMOS, ECL, 10H, ECLinPS, ECLinPS Lite, PLL, and biCMOS. Revision 3 of the data book contains updates on the company's low-voltage and 5-V PLL clock drivers, low-voltage/low-skew fanout buffers, and clock-generation circuits. Data sheets as well as application notes on circuit-design considerations, clock-distribution techniques, and designing with PECL are included. DM **CIRCLE 943**

BIG ENCLOSURE BOOK IN PRINT OR ON DISK

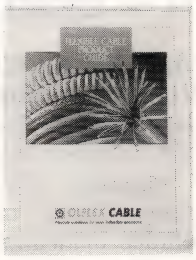


Modular cabinets, sloped-front cabinets, electronic desks, computer furniture, and instrument cabinets are described in a 316-page catalog from Equipto Electronics Corp., Aurora, Ill. The catalog, which is available in print or on disks for DOS-compatible machines, features technical sections with schematic drawings and complete dimensions. Included is a section on EMI/RFI-shielded enclosures that meet FCC and TEMPEST requirements. DM **CIRCLE 944**

BIG DATABOOK COVERS MCTs, IGBTs, DIODES

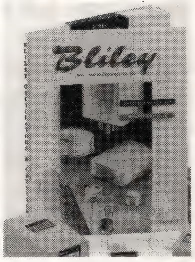
MOS-controlled thyristors (MCTs), insulated-gate bipolar transistors (IGBTs), and general-purpose and high-speed diodes are all covered in a 512-page databook from Harris Semiconductor, Melbourne, Fla. The book provides long-form data sheets and extensive application and general information. Sections include MCTs, IGBTs, general-purpose diodes, ultrafast and hyperfast single and dual diodes, application notes, quality and reliability information, and packaging and ordering information. DM **CIRCLE 945**

FLEXIBLE CABLE FEATURED IN GUIDE



Divided into easy-to-read sections, a flexible-cable product guide outlines the cable line from Olflex Wire & Cable Inc,. Fairfield, N.J. Cables for all factory-automation applications are offered including continuous-flex, oil-resistant types; oil-resistant flexible control cables; harmonized flexible cords and hook-up wire for use in Europe; Unitronic cables for use in North America and Europe; spiral cables; and cables for conveyor systems. Pertinent specifications and applications for each product category are provided. DM **CIRCLE 946**

CRYSTAL CATALOG IS EASY ON THE EYES

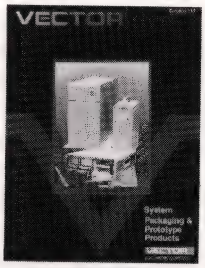


A reader-friendly format is a hallmark of a 20-page catalog of quartz crystals and oscillators from Bliley Electric Co., Erie, Pa. Catalog C/F_2 presents color-keyed product categories with each type introduced by feature and application highlights. Crystal oscillators are shown in separate sections devoted to oven-controlled, temperature-compensated, voltage-controlled, and clock-oscillator types. Each is illustrated with photos and dimensional drawings. Quartz crystals are similarly presented in a full array that includes cold-weld and ultra-high stability versions. A plastic binder keeps the catalog neat and gives it high visibility. DM **CIRCLE 947**

FIBER-OPTIC PRODUCTS CATALOG

A 132-page catalog from Molex Fiber Optic Interconnect Technologies, Lisle, Ill., features performance information and technical specifications on the company's full line of fiber-optic connectors and adapters, as well as its cable assemblies, termination tooling, fiber-optic switches, and premise wiring products. In addition, the catalog features a glossary and a special section that describes connector-termination procedures, including the tooling required. CM **CIRCLE 948**

ALL-LINE CATALOG

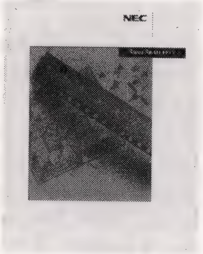


The All-Line Catalog 112 from Vector Electronic Company, Sylmar, Calif., includes drawings, photos, dimensions, and other technical information on Vector's complete line of system enclosures, backplanes, subracks, Vectorbord prototype boards, card cages, printed-circuit board connectors, and PCB accessories, such as press-in terminals, socket pins, and wire-wrapping tools. The 136-pagecatalogisfree. CM **CIRCLE 949**

NO CLEAN SOLDER PASTES

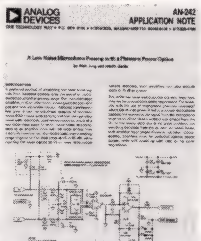
"No Clean SMT Solder Pastes...A Practical Guide" is a 12-page, illustrated, full-color primer from Heraeus Inc., Cermalloy Division, Sellersville, Pa., on how to evaluate, select, and get the best performance from No Clean solder pastes. Designed to provide generic, detailed information to all pc-board assemblers who must eliminate CFC-bearing solvent-clean solder pastes from their operations, the guide explains what a no clean paste is, and whether or not it can be used as a drop-in replacement for solvent clean. The guide recommends what to look for when evaluating the various types of no clean solder pastes, including standard, low residue, and ultra-low residue. It also discusses air versus nitrogen reflow, and makes general recommendations on the reflow profile that should be achieved with a no clean paste. Also covered is testing, with a summary of typical standard tests that must be performed to properly evaluate a solder paste's performance, including "real world" testing on the prospective user's line. The guide is free. CM **CIRCLE 950**

SMALL-SIGNAL FETS SELECTION GUIDE



A six-page product selection guide from California Eastern Labs, Santa Clara, Calif., covers NEC's range of small-signal GaAs FET products: low-noise GaAs FETs, general-purpose GaAs FETs, and dual-gate GaAs FETs. The guide provides an easy-to-use overview of the key electrical characteristics and package dimensions. CM **CIRCLE 951**

LOW-NOISE MICROPHONE PREAMP



Application note AN-242, "A Low Noise Microphone Preamp with a Phantom Power Option," from Analog Devices, Wilmington, Mass., describes the design and application of a high-performance two-IC microphone preamp. A schematic diagram is included, as well as considerations for obtaining optimum sonic performance. The combined features of Analog Devices' SSM-2017 differential input audio IC and OP-275 dual bipolar/JFET low-noise op amp are shown in this circuit used for a variable gain microphone preamp with optional phantom power.

Phantom power allows users to remotely power condenser microphones, preamps, and active direct boxes on the same wires that are used to carry the audio signal. Radio frequency interference, as a potential problem for high-gain preamps, is investigated. Also, output control and performance are discussed. Gain and noise performance of the two-chip preamplifier are graphed. CM **CIRCLE 952**

WIRE-TRACKING ADHESIVES GUIDE

An application selector guide fron Master Bond Inc., Hackensack, N.J. features an extensive line of high performance adhesive compound for tacking wires and attaching components to printed-wiring boards These adhesives are designed to offer technically superior and cost-effective solutions for a variety of attachment problems. One- and two component epoxies, UV-curable epoxies, reactive acrylics, hot melt, anc cyanoacrylate adhesives are illustrated. Application conditions anc performance profiles are providec for each type of product. Special attention is paid to both ease and speec of application. Adhesives shown offer superior resistance to severe environmental conditions, including thermal cycling, shock and vibration, and high humidities. CM **CIRCLE 953**

MULTI-PIN CONNECTORS DISCONNECT QUICKLY

A 44-page catalog from Contact Electronics Inc., Fairfield, N.J., details the Epic line of NEMA-4-rated connectors for all power and control applications where reliability and durability are essential. The connectors allow for quick disconnection of signal and power lines between various electrical components throughout a control system or automated machinery. Crimp or screw terminations are offered in from 3 to 216 contacts with rugged housings that withstand severe environments. The catalog contains complete technical information, photos, dimensional diagrams, and many charts and tables designed to help select the proper connector for a given application. DM **CIRCLE 954**

CATALOG FEATURES TRANSDUCERS, BUZZERS

A new brochure details all the pertinent features and applications of the full line of audio transducers and buzzers from Star Micronics America, Piscataway, N.J. The 33-page, four-color catalog features brief summaries and photographs of all the products and fully describes all the components with easy to read graphs and diagrams. The catalog is free. CM **CIRCLE 955**

UPCOMING MEETINGS

JUNE

Applied Machine Vision '94, June 6-9. Sheraton Park Place, Minneapolis, MN. Contact Lisa Moody, Society of Manufacturing Engineers, 1 SME Dr., Box 930, Dearborn, MI 48121-0930; (313) 271-1500.

31st Design Automation Conference, June 6-10. San Diego Convention Center, San Diego, CA. Contact 31st Design Automation Conference, Attn.: Registration Desk, 5305 Spine Rd., Suite A, Boulder, CO 80301; (303) 530-4333; fax (303) 530-4334.

INFOCOM '94, June 12-16. Westin Harbour Castle, Toronto, Ontario, Canada. Contact Mark J. Karol, AT&T Bell Labs, Room 4F-529, 101 Crawfords Corner Rd., Holmdel, NJ 07733-3030; (908) 949-8590; fax (908) 949-9118; E-mail: mk@boole.att.com.

Society for Information Display, International Symposium Seminar & Exhibition (SID '94), June 12-17. San Jose Convention Center, San Jose, CA. Contact Joyce E. Farrell, SID '94 Conference Chair, Hewlett-Packard Laboratories, P.O. Box 10490, Palo Alto, CA 94303-0969; (415) 857-2807; fax (415) 857-4320; E-mail: Farrell@hplabs.hp.com.

CSI's NetSec '94, Network Security in the Open Environment, June 13-15. Sheraton Palace, San Francisco, CA. Contact CSI Conference Registration, 600 Harrison St., San Francisco, CA 94107; (415) 905-2626; fax (415) 905-2218.

DSPX Conference & Exposition, June 13-15. Moscone Convention Center, San Francisco, CA. Contact DSPX Customer Service, (203) 352-8289.

Computer Modeling of Optical Waveguides and Components: A Hands-on Workshop, June 14-17. National Institute of Standards and Technology, Boulder, CO. Contact R.L. Gallawa, U.S. Dept. of Commerce, National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80303-3328; (303) 497-3761, fax (303) 497-3387.

IEEE Conference on Computer Vision & Pattern Recognition, June 20-24. The Westin Hotel, Seattle, WA. Contact IEEE Computer Society, Conference Dept., 1730 Massachusetts Ave. NW, Washington D.C. 20036-1992; (202) 371-1013, fax (202) 728-0884.

IEEE Antennas & Propagation Society International Symposium & URSI National Radio Science Meeting, June 20-24. University of Washington, Seattle, WA. Contact Akira Ishimaru, University of Washington, Dept. of Electrical Engineering, FT-10, Seattle, WA 98195; (206) 543-2169.

International Conference on Applications of Photonic Technology Sensing, Signal Processing & Communications (ICAPT), June 21-23. Hilton International Hotel, Toronto, Ontario, Canada. Contact George A. Lampropoulos, A.U.G. Signals Ltd., 560 Lauder Ave., Toronto, Ontario, M6E 3J6, Canada; (905) 658-6353; fax (905) 654-6310; E-mail: lampro@utcc.gpu.utoronto.ca.

European Fibre-Optic Communications & Networks, June 22-24. Heidelberg, Germany. Contact Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA; (617) 232-3111; fax (617) 734-8562.

IEEE 3rd International Fuzzy Systems Conference, June 26-29. Walt Disney World Dolphin Hotel, Lake Buena Vista, FL. Contact Steve Marlin, Meeting Management Inc., 2603 Main St., Suite 690, Irvine, CA 92714; (714) 752-8205; fax (714) 752-7444.

9th Conference on Computer Assurance (Compass '94), June 27-July 1. National Institute of Standards and Technology, Gaithersburg, MD. Contact John McLean, (202) 767-3852; fax (202) 404-7942.

Conference on Precision Electromagnetic Measurements (CPEM '94), June 27-July 1. Clarion Harvest House Hotel, Boulder, CO. Contact Donald B. Sullivan, Div. 847, National Institute of Standards and Technology, Boulder, CO 80303-3328; (303) 497-3772.

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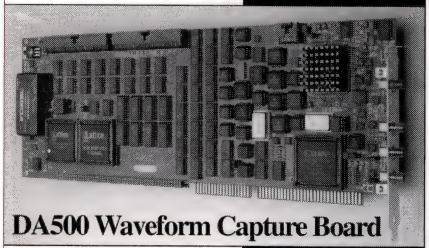

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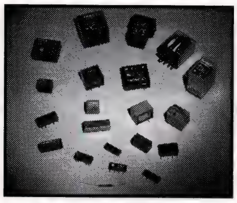

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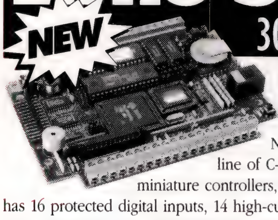

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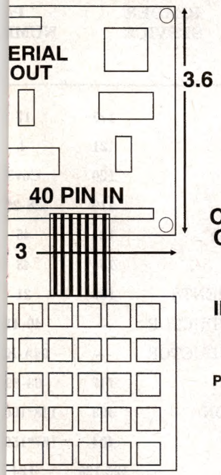

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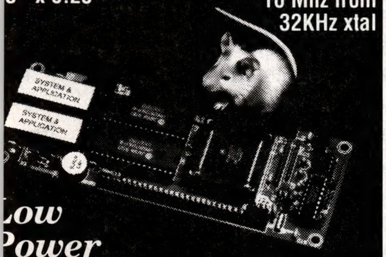

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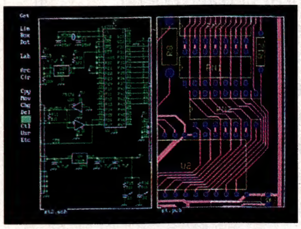

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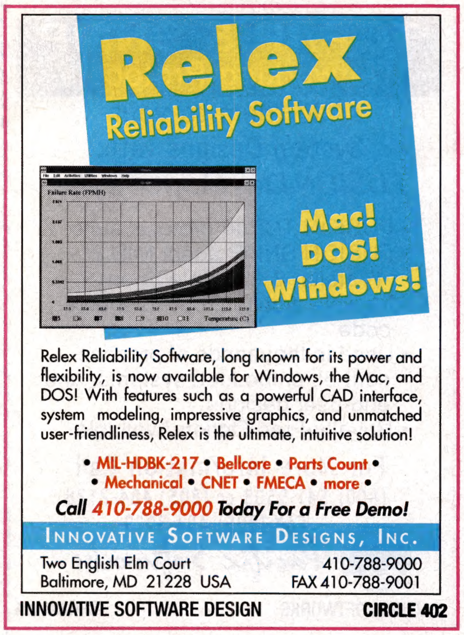

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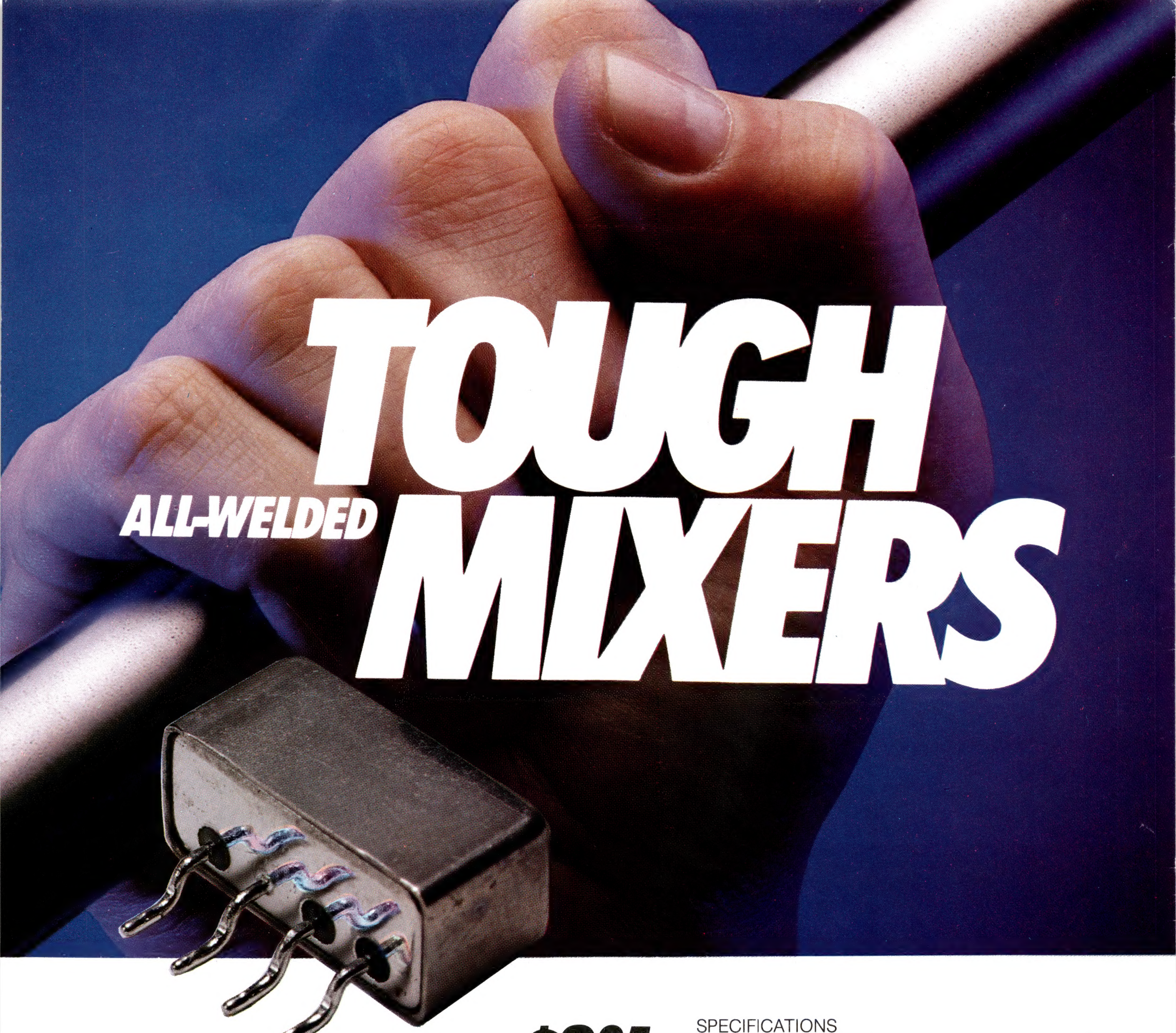

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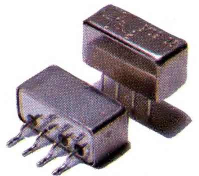
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Model	LO Power (dBm)	Freq. LO/RF (MHz)	■ Conv. Loss (dB)		Isol. L-R (dB)	Price,$ Ea. 10 qty
			$\overline{X}$	δ		
TUF-3	7	0.15-400	4.98	0.34	46	5.95
TUF-3LH	10		4.8	0.37	51	7.95
TUF-3MH	13		5.0	0.33	46	8.95
TUF-3H	17		5.0	0.33	50	10.95
TUF-1	7	2-600	5.82	0.19	42	3.95
TUF-1LH	10		6.0	0.17	50	5.95
TUF-1MH	13		6.3	0.12	50	6.95
TUF-1H	17		5.9	0.18	50	8.95
TUF-2	7	50-1000	5.73	0.30	47	4.95
TUF-2LH	10		5.2	0.3	44	6.95
TUF-2MH	13		6.0	0.25	47	7.95
TUF-2H	17		6.2	0.22	47	9..95
TUF-5	7	20-1500	6.58	0.40	42	8.95
TUF-5LH	10		6.9	0.27	42	10.95
TUF-5MH	13		7.0	0.25	41	11.95
TUF-5H	17		7.5	0.17	50	13.95
TUF-860	7	860-1050	6.2	0.37	35	8.95
TUF-860LH	10		6.3	0.27	35	10.95
TUF-860MH	13		6.8	0.32	35	11.95
TUF-860H	17		6.8	0.31	38	13.95
TUF-11A	7	1400-1900	6.83	0.30	33	14.95
TUF-11ALH	10		7.0	0.20	36	16.95
TUF-11AMH	13		7.4	0.20	33	17.95
TUF-11AH	17		7.3	0.28	35	19.95

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■ $\overline{X}$ = Average conversion loss at upper end of midband ($f_U/2$)
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